Himax Display, Inc.

DATA SHEET

(DOC No. HX7027ATGFA-DS)

HX7027ATGFA

640X480 0.44” LCOS Module

version 3.0 July, 2008

Himax Display, Inc.
http://www.himaxdisplay.com

Revision History

Version	Date	Author	Description of Changes
01	2007/06	CJ	New setup
1.0	2008/01	Nikai, Tiggy	1.MP specification 2.Add optical characteristics. 3.Add level information
2.0	2008/04	Linda	1.Modify label shipping quantity to correct number
3.0	2008/07	Linda	1.Datasheet cover change new version 2.Modify 13.1 packing procedure 3.Update 11.3 panel reflection spectrum drawing 4.LTS Test change from -20℃ to -40℃

Contents

1. About This Document

This document validates solely for the product of Himax Display, HX7027ATGFA. However, this document is not fully complete yet, therefore, this datasheet only provides basic information and electronic characteristics. This document is for customer’s reference only, and it subjects to change without notice.

Note: HX7027ATGFA is already under Mass production.

2. General Description

HX7027ATGFA is an active matrix liquid crystal display with resolution of 640X480XRGB dots. HX7027ATGFA is ideal for portable and industrial applications. Horizontal digital data drivers and vertical scan drivers are integrated with single crystal pixel transistors meet the performance demands of light weight, high speed and high resolution applications. HX7027ATGFA receives 8-bits x 3-dots (RGB) of digital display data per clock simultaneously and generates corresponding voltage output of 256 level gray scales, which displays 16M colors simultaneously.

3. Features

- Resolution of 640x480x3
- No spacers in the display area.
- RGB 8-bit digital inputs.
- Integrated horizontal data and vertical scan drivers.
- Horizontal and vertical bi-directional scanning.
- Embedded DE mode timing controller.
- Maximum 15V power input
- Capable of displaying 256 gray scales by 12 internal γ reference voltages.
- Embedded programmable gamma reference voltages.
- Embedded programmable VCOM voltage
- Two-wire serial interface for internal register setting.

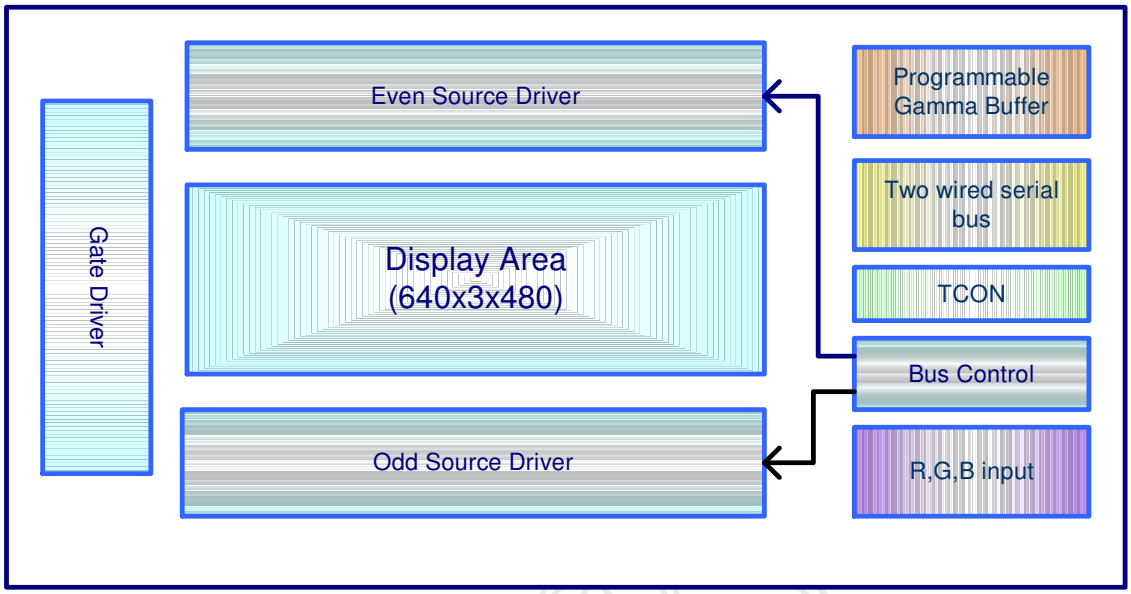
4. Quick Reference Data

Parameter	Specification	Unit
Size of Display (Diagonal)	0.44”	inch
Active Area Dimensions	8.832 X 6.624	mm
Native Area Dimensions	8.832 X 6.624	mm
Display Resolution	640X480X3	pixels
Aspect Ratio	4:3	-
Pixel Pitch (X, Y)	13.8X13.8	μm
Pixel Configuration	Delta	-
Gray Level	256 (8-bits)	-
Contrast ratio @ F/2.5	100	%
Optical Efficiency: Reflectance	19 (Note 1)	%
Optical Mode	Reflective	-
Liquid Crystal Mode	Twisted Nematic	-
Operation Mode	Normally White	-
Response Time (Tr+Tf)	15	ms
Operating Temperature	0~50	℃
Mechanical Characteristics	Chap. 15	-
Weight	4	g
Scrolling	No	-

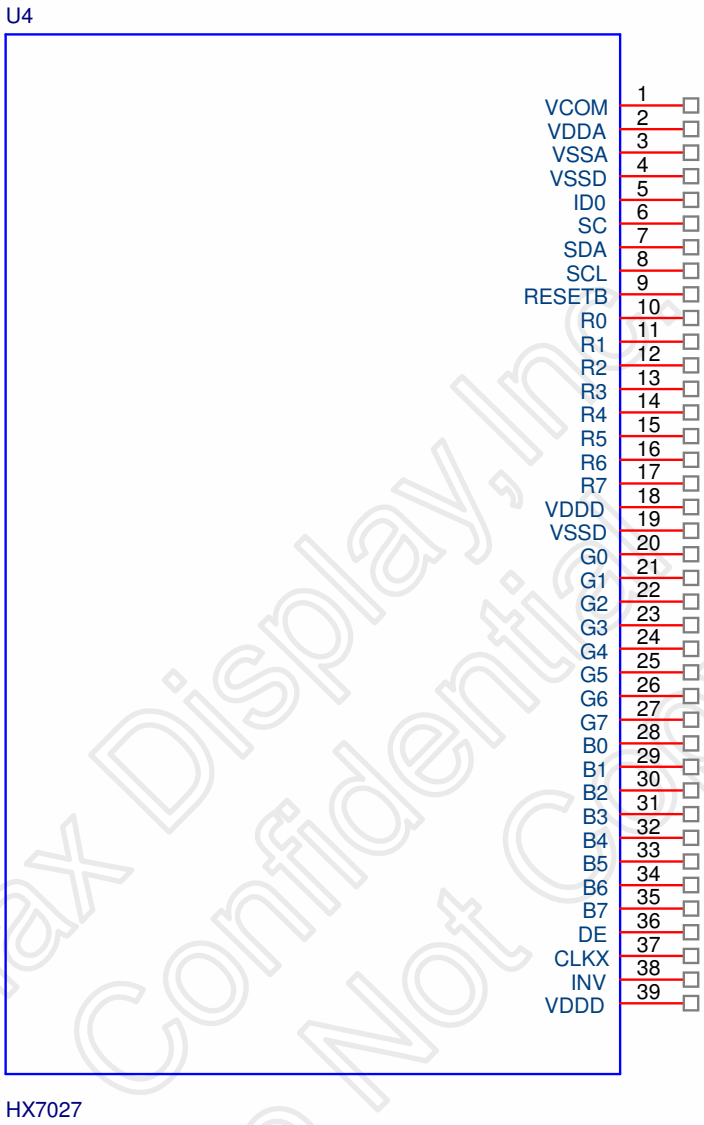
All values specified at a display ambient temperature of 25℃.

Note 1: For light with wavelength from 430mm to 650mm

5. Block Diagram



6. Pin Assignment



7. Pin Description

Pin name	I/O	Function	Description
R0~R7 G0~G7 B0~B7	I/O	TTL display data input	The display data is input in 8-bit × 3 dots (RGB) per CLK clock. For each input dot, X0 is LSB and X7 is MSB.
DE	I	Display active	
CLKX	I	X-axis shift clock input	The display data is stored to the internal data register at the rising edge of CLKX.
RESETB	I	Reset panel	Reset the panel when RESETB=0. Set RESETB=1 during normal operation.
SC	I	Single cell	When SC=VDDD, all pixel voltage is charged to “VCOM”. Default internal 50K ohm resistor connecter to GND.
SDA	I/O	Two-wire serial interface Data I/O	Serial data I/O
SCL	I	Two-wire serial interface Clock input	Input clock for serial bus.
ID0	I	Two-wire serial interface address 0	LSB address for serial bus.
VDDA	I	Driver power supply	15V
VSSA	I	Driver ground	Ground for VDDA
VDDD	I	Logic power supply	3.3V±0.3V
VSSD	I	Logic ground	Ground for VDDD
VCOM	O	Top glass voltage for Liquid Crystal	Connect 0.1uF capacitor to GND.

8. Function Description

This section describes about the following topics:

- Input Timing
- Relationship between input data and output position
- Relationship between input data and output voltage
- γ correction characteristic curve
- Digital to Analog Converter
- Serial Interface
- Details of read/write sequence of 2-wired serial bus

8.1 Input Timing

Description	Min.	Typ.	Max.	Unit
Horizontal Total	680	800	880	Pixel
Horizontal Display	--	640	--	Pixel
Horizontal Blanking	40	160	240	Pixel
Vertical Total	485	525	--	Line
Vertical Display	--	480	--	Line
Vertical Blanking	5	45	--	Line
Frame rate	85	120	--	Hz
Pixel Clock	--	50	--	MHz

8.2 Relationship between Input Data and Output Position

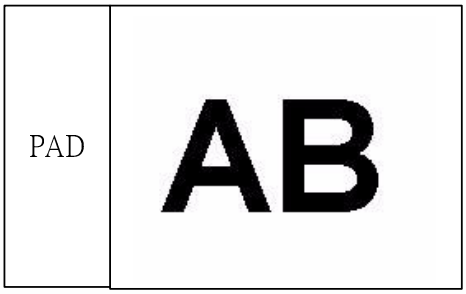
Input data format: 8-bit × 3 (3 dots per CLK)
Input data width: 24 bits (1 pixels data) with X7 is MSB and X0 is LSB

RL	first			→	last		
	R0~R7	G0~G7	B0~B7	•••	R0~R7	G0~G7	B0~B7
"H"	OUT0			•••	OUT639		

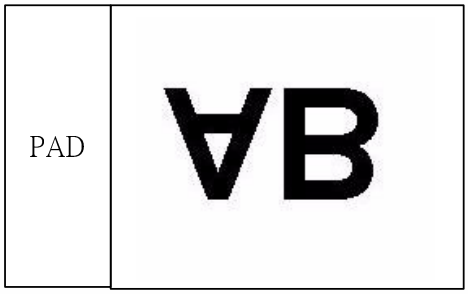
RL	last			←	first		
	R0~R7	G0~G7	B0~B7	•••	R0~R7	G0~G7	B0~B7
"L"	OUT639			•••	OUT0		

The following pictures show the final display results when adjusts the UD and RL.

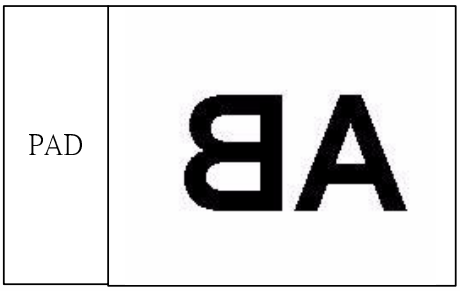
UD=0, RL=0



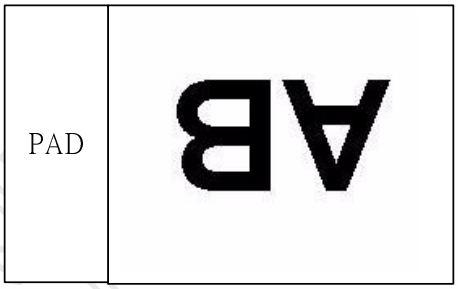
UD=1, RL=0



UD=0, RL=1



UD=1, RL=1

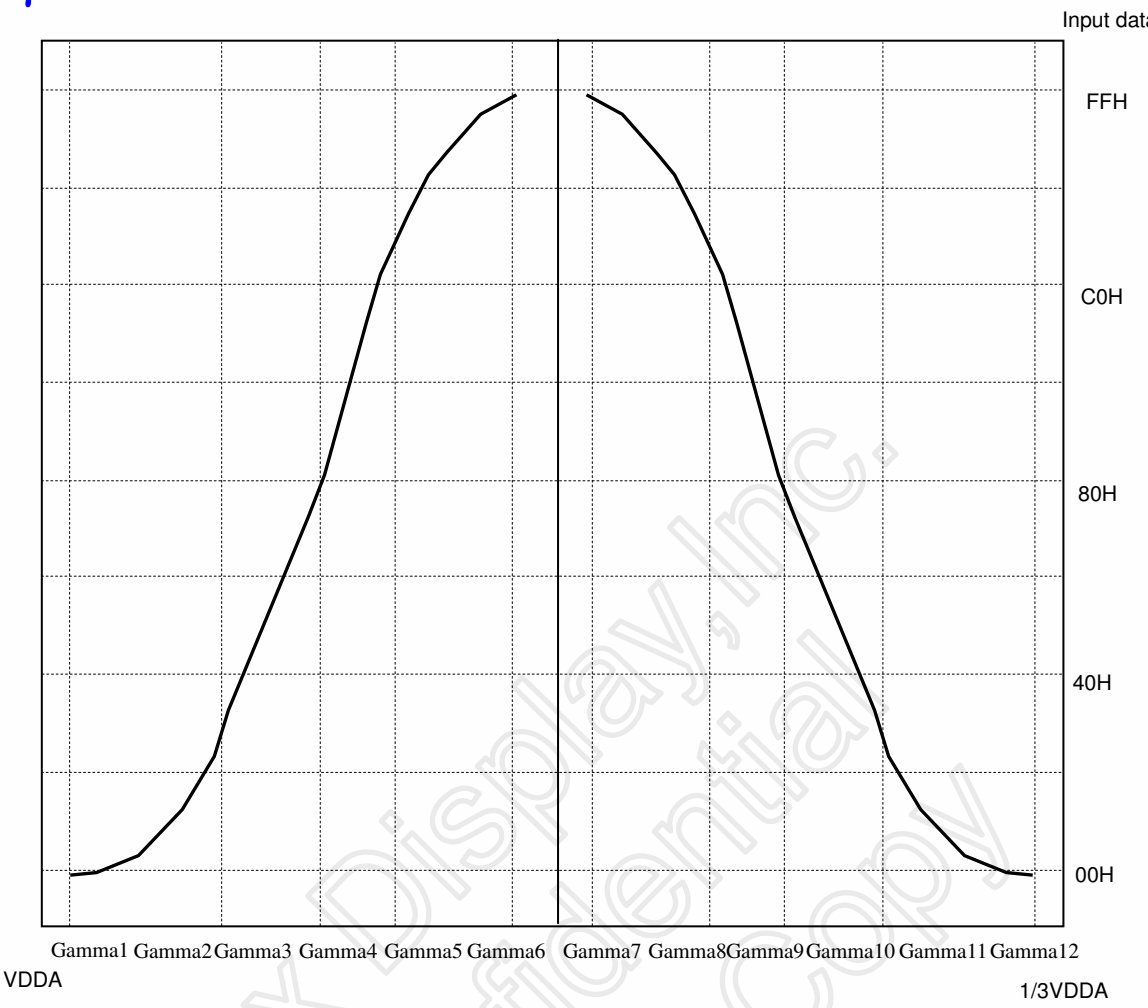


8.3 Relationship between Input Data and Output Voltage

The output voltage is determined by these 8-bit digital input data, internal signal “POL”, and the 6 γ correction reference voltage. Through 6 embedded γ correction reference voltage, Gamma1 ~ Gamma6 are for positive polarity voltage output, and embedded voltage Gamma7 ~ Gamma12 are for negative polarity voltage output.

Gamma Voltage	Data
Gamma1, Gamma12	00H
Gamma2, Gamma11	3FH
Gamma3, Gamma10	7FH
Gamma4, Gamma9	BFH
Gamma5, Gamma8	FBH
Gamma6, Gamma7	FFH

8.4 γ Correction Characteristic Curve



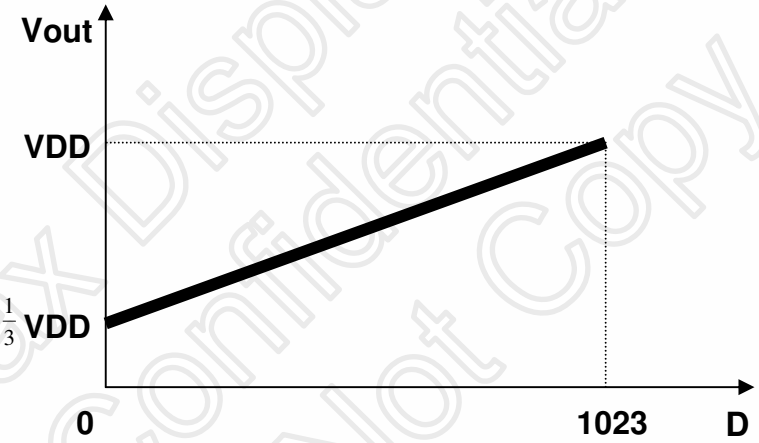
8.5 Digital to Analog Converter

HX7027ATGFA contains 12 DACs with resolution of 10 bits. Each bit contains output buffer amplifiers and is written via a two-wire serial interface. They operate from power supplies of 5V to 15V and the output buffer amplifiers provide rail-to- rail output. All DAC are provided with reference input. The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the VDDA pin provides the high reference voltage for the corresponding DAC. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{out} = \frac{\frac{2}{3}VDDA * D}{2^N - 1} + \frac{1}{3}VDDA$$

Where

D = decimal equivalent (0~1023) of the binary code that is loaded to the DAC register; *N* = 10



8.6 Serial Interface

HX7027ATGFA is controlled via a two wire serial interface. The device is connected to this bus as slave devices. HX7027ATGFA has a 7-bit slave address. There are six MSBs as 100100, and a LSB. LSB are determined by the state of the ID0 pins. Users are able to change slave address through 2-wire serial interface by modifying ID0. (Refer to chapter 8.7 Details of read/write sequence of 2-wired serial interface).

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7th bit slave address followed by an R/*W* bit (this bit determines whether data will be read from or written to the slave device).

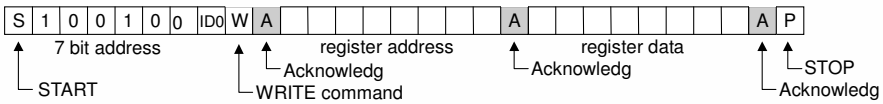
The slave whose address corresponds to the transmitted address responds by pulling SDA low during the 9th clock pulse (this is the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

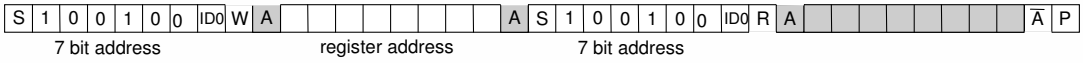
3. When all data bits have been read or written to, a STOP condition is established. In Write/Read mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

8.7 Details of Read/Write Sequence of 2-Wired Serial Interface

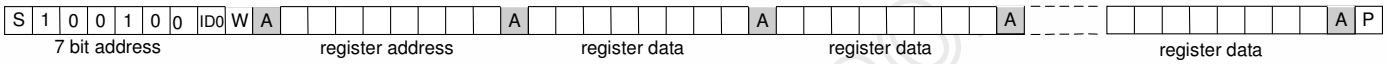
Random Write Operation



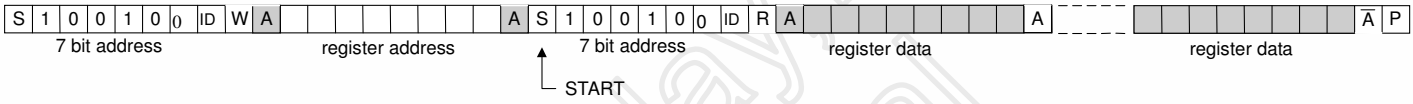
Random Read Operation



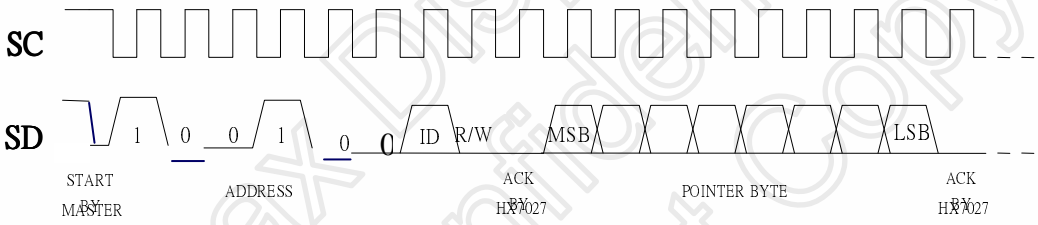
Page Write Operation



Page Read Operation



Direction: From master to device From device to master Note: R=READ=1 and W = Write =0



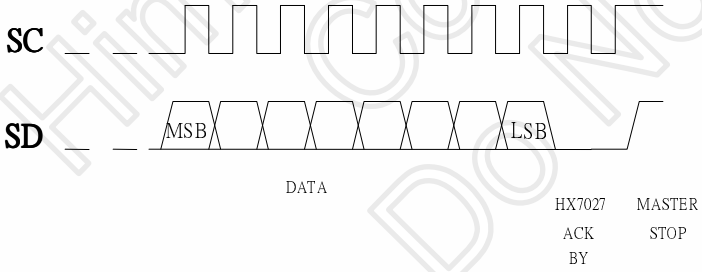


Table 8.1: Description of 2-Wired Serial Interface Register

I2C register	ADDR.	DATA.	register default value	note
	[00]h	[x , x , x , x , VGA , UD , LR , SC_I2C] h	[0 , 0 , 0 , 0 , 1 , 1 , 1 , 0]	control setting
	[01]h	[x , CLK_POS , DTREN , TCON , TCON_OUT , POL_INV , OSC_O_EN , TEST_XY] h	[0 , 1 , 1 , 1 , 0 , 0 , 0 , 0]	control setting
	[02]h	[PF_RV1 , PF_RV1B , PF6 PF5 , PF4 , PF3 , PF2 , PF1] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	control setting
	[03]h	[A7 , A6 , A5 , A4 , A3 , A2 , PF_VCOM , PF_PT] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	control setting
Gamma1	[04]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 1]	gamma1 code
	[05]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 1 , 0 , 1 , 1 , 1 , 0 , 1]	14.667V (989)
Gamma2	[06]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 1]	gamma2 code
	[07]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 1 , 0 , 0 , 0 , 1 , 0 , 1]	13.18500V (837)
Gamma3	[08]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 1]	gamma3 code
	[09]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 1]	12.52V (769)
Gamma4	[0a]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 0]	gamma4 code
	[0b]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 1 , 0 , 0 , 1 , 0 , 0 , 1]	11.97V (713)
Gamma5	[0c]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 0]	gamma5 code
	[0d]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 1 , 1 , 1 , 1 , 1 , 0 , 1]	11.228V (637)
Gamma6	[0e]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 1 , 0]	gamma6 code
	[0f]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 0 , 0 , 1 , 0 , 1 , 0 , 0]	10.2V (532)
Gamma7	[10]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 1]	gamma7 code
	[11]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 1 , 0 , 1 , 0 , 1 , 1 , 1]	9.6V (471)
Gamma8	[12]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 1]	gamma8 code
	[13]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 1 , 1 , 0 , 1 , 1 , 0 , 1]	8.572V (365)
Gamma9	[14]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 1]	gamma9 code
	[15]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 0 , 1 , 0 , 0 , 0 , 0 , 1]	7.83V (289)
Gamma10	[16]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	gamma10 code
	[17]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 1 , 1 , 0 , 1 , 0 , 0 , 1]	7.28V (233)
Gamma11	[18]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	gamma11 code
	[19]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 0 , 1 , 0 , 0 , 1 , 0 , 1]	6.615V (165)
Gamma12	[1a]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	gamma12 code
	[1b]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 0 , 0 , 0 , 1 , 1 , 0 , 1]	5.133V (13)
VCOM	[1c]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 1]	VCOM code
	[1d]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[1 , 1 , 1 , 1 , 0 , 1 , 0 , 1]	9.90V (501)
	[1e]h	[x , x , x , x , x , x , A9 , A8] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	backup reg
	[1f]h	[A7 , A6 , A5 , A4 , A3 , A2 , A1 , A0] h	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	backup reg

Table 8.2: Description of 2-Wired Serial Interface Default Register

Default Setting/ Description	Note
VGA = 1, VGA mode;	
UD = 1, display up to down	
LR = 1, display left to right	
SC_I2C = 0, single cell disable	
CLK_POS = 1, input CLK positive edge sample	
DTREN = 1, dithering enable	
TCON = 1, enable TCON	Reserve for test mode. It must be set to 1 in normal mode.
TCON_OUT=1, internal TCON out	Reserve for test mode.
POL_INV=0, POL inversion	Reserve for test mode. It must be set to 0 in normal mode.
TEST_XY=0, default TEST_Y out	Reserve for test mode.
OSC_O_EN = 1 , osc clk out	Reserve for test mode.
PF_RV1 = 0 , RV on	Reserve for test mode. It must be set to 0 in normal mode.
PF_RVB1 = 0 , RVB on	Reserve for test mode. It must be set to 0 in normal mode.
PF[6:1] = 0 , Gamma[6:1] on	Reserve for test mode. It must be set to 0 in normal mode.
PF_PT = 0 , bandgap on	Reserve for test mode. It must be set to 0 in normal mode.

Gamma Reference Voltage / Code	
gamma1 = 14.667V	[11-1101-1101]
gamma2 = 13.185V	[11-0100-0101]
gamma3 = 12.520V	[11-0000-0001]
gamma4 = 11.970V	[10-1100-1001]
gamma5 = 11.228V	[10-0111-1101]
gamma6 = 10.200V	[10-0001-0100]
gamma7 = 9.600V	[01-1101-0111]
gamma8 = 8.572V	[01-0110-1101]
gamma9 = 7.830V	[01-0010-0001]
gamma10 = 7.280V	[00-1110-1001]
gamma11 = 6.615V	[00-1010-0101]
gamma12 = 5.133V	[00-0000-1101]
VCOM = 9.90V [01-1111-0101]	

9. DC Characteristics

This section describes about the following topics:

- Absolute Maximum Rating
- Recommended Operating Conditions
- Electrical Characteristics

9.1 Absolute Maximum Ratings

Parameter	Symbol	Rating			Unit
Power supply voltage	VDDA	-0.5	to	+15	V
	VDDD	-0.5	to	+3.6	V
Input voltage	CMOS/TTL Input	-0.5	to	VDDD	V

Note: The Device is subjected to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

9.2 Recommended Operating Conditions

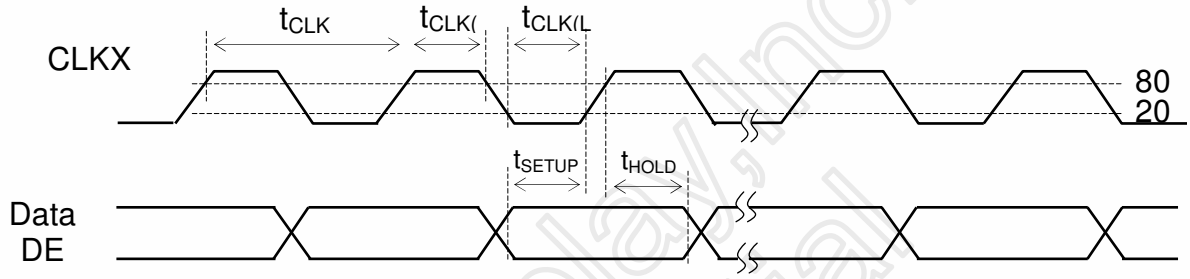
Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDA	12		15	V
	VDDD	3.0	3.3	3.6	V
γ correction reference voltage	V_1 ~ V_{12}	$\frac{1}{3}$ VDDA		VDDA-0.1	V
Input capacitance	Cin				pF
Operation frequency	f_{CPV}		50		MHz

9.3 Electrical Characteristics

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
High level input voltage	VIH	R0~R7, G0~G7, B0~B7, CLKX, DE, SC,INV, ID0, RESETB	0.7×VDDD		VDDD	V
Low level input voltage	VIL		0		0.2×VDDD	
Input leak current	IL		-1		1	μA
VDDD static current	IVDDD	DE=CLK=R[7:0] =G[7:0]=B[7:0]=R ESETB=INV=ID0 = VDDA=0 V		5		μA

10. AC Characteristics

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Clock pulse width	t_{CLK}			20		ns
Clock pulse low period	$t_{CLK(L)}$		8			ns
Clock pulse high period	$t_{CLK(H)}$		8			ns
Data & DE setup time	t_{SETUP}		4			ns
Data & DE hold time	t_{HOLD}		4			ns



11. Optical Characteristics

Reflective twisted-nematic liquid crystal mode is employed in HX7027. When no voltage is applied, HX7027 presents bright state (i. e. the normally white mode). The images darken up as the applied voltage increases. Different gray-level can be obtained by tuning the applied voltage

HX7027 is a color-filter-inside (CF-LCOS) design that exhibits color images by single panel.

11.1 Optical Specifications

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±5	℃
Ambient Humidity	Ha	50±20	%RH
Supply Voltage	Vdda	15±0.3	V
Input Signal	According to typical value in "ELECTRICAL CHARACTERISTICS"		

11.2 Optical Specifications

Item			Condition	Min.	Typical	Max.	Unit	Notes
Reflectance			%(430~650nm) @F/2.5	17	19		%	Note 1
Uniformity of Reflectance			Measure VESA 9 pts as figure	80	-		%	Note 2
Contrast Ratio			Full white/black @F/2.5	80	110		-	Note 3
Chromaticity	**R**	**x**	Unity light source	0.525	0.565	0.605	-	Note 4
		y		0.285	0.325	0.365		
	G	**x**		0.245	0.285	0.325		
		y		0.485	0.525	0.565		
	B	**x**		0.115	0.155	0.195		
		y		0.14	0.18	0.22		
	W	**x**		0.3	0.34	0.38		
		y		0.34	0.38	0.42		
Response Time	**T_R**		Full bright to dark		2	5	ms	Note 5
	T_F		Full dark to bright		8	13	ms	
	gray to gray average		Gray scale 6x6 matrix		10	15	ms	

PS. All values are measured the normal direction to the panel.

Note 1: Definition of Reflectance：

Reflectance is measured by MDIS (Westar Inc.)
Measure the Reflectance of gray scale 255 at center point.
Figure 1.1 shows the optic measurement system of MDIS.
Figure 1.2 shows the polarization direction of incident light.

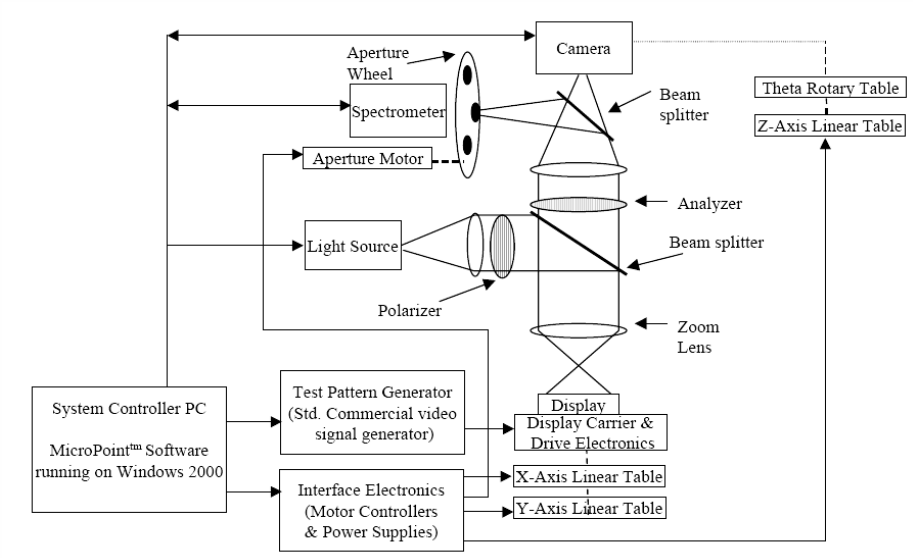


Figure 1.1 MDIS optic measurement system

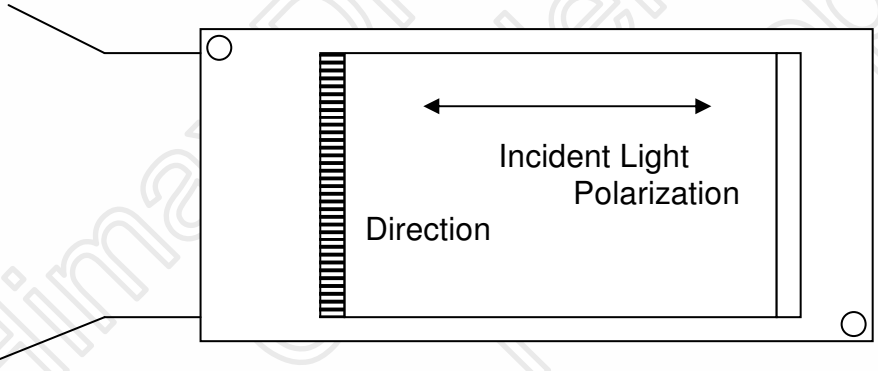
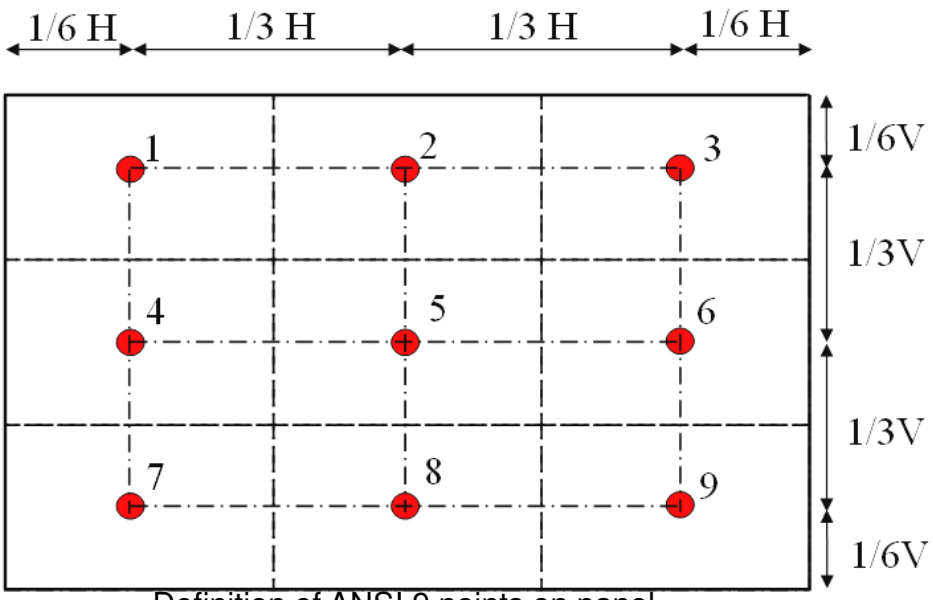


Figure 1.2 Polarization direction of incident light

Note 2: Definition of Uniformity of Reflectance
Measure the luminance of gray 255 at 9 points by MDIS.
Uniformity = Minimum[L(1),L(2),L(3),L(4),L(5),L(6),L(7),L(8),L(9)] /
Maximum[L(1),L(2),L(3),L(4),L(5),L(6),L(7),L(8),L(9)]



Definition of ANSI 9 points on panel

Note 3: Definition of Contrast Ratio:
Luminance of gray 255 and gray 0 are measured by MDIS at the center point.
The contrast ratio is calculated by the following expression.
CR=L255/L0
PS. 1. L255= Luminance of gray level 255
2. L0= Luminance of gray level 0

Note 4: Definition of Chromaticity
WRGB reflection spectrums were measured by MDIS (Westar Inc.)
The color chromaticity values are calculated by assuming an equal intensity visible waveband (430nm~650nm) light source.

Note 5: Definition of Response Time (T_R and T_F)
Measured by HIMAX DISPLAY photo diode sensor & oscilloscope under temperature 45℃.
Figure 5.1 Definitions of T_R and T_F
Figure 5.2 Definition of gray to gray switching time

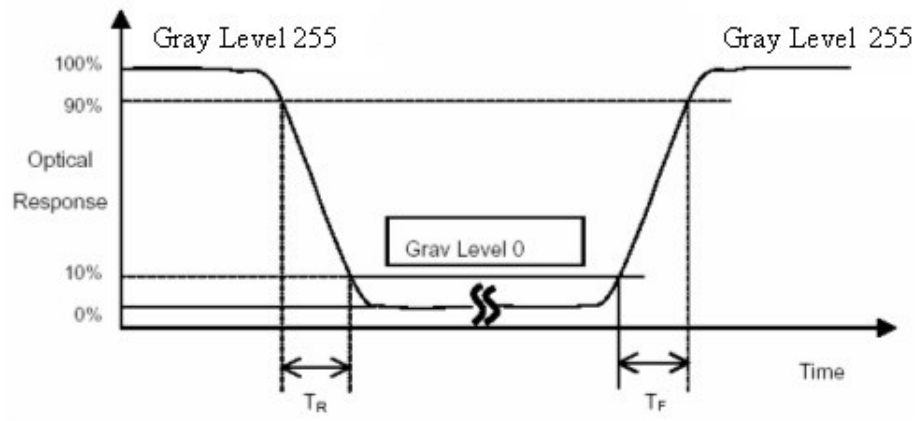


Figure 5.1 Definition of T_R and T_F

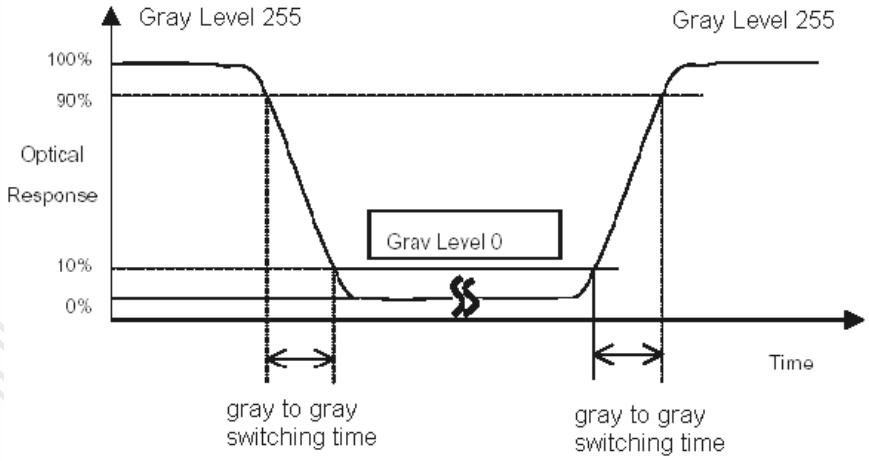
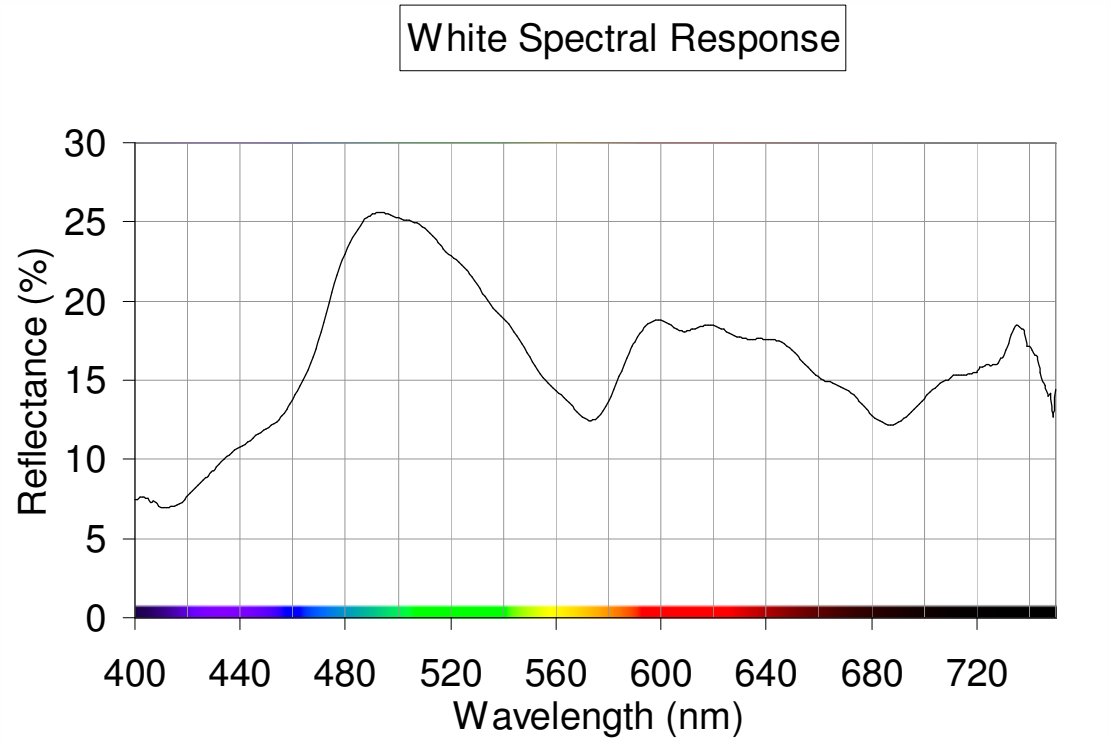


Figure 5.2 Definition of gray to gray switching time

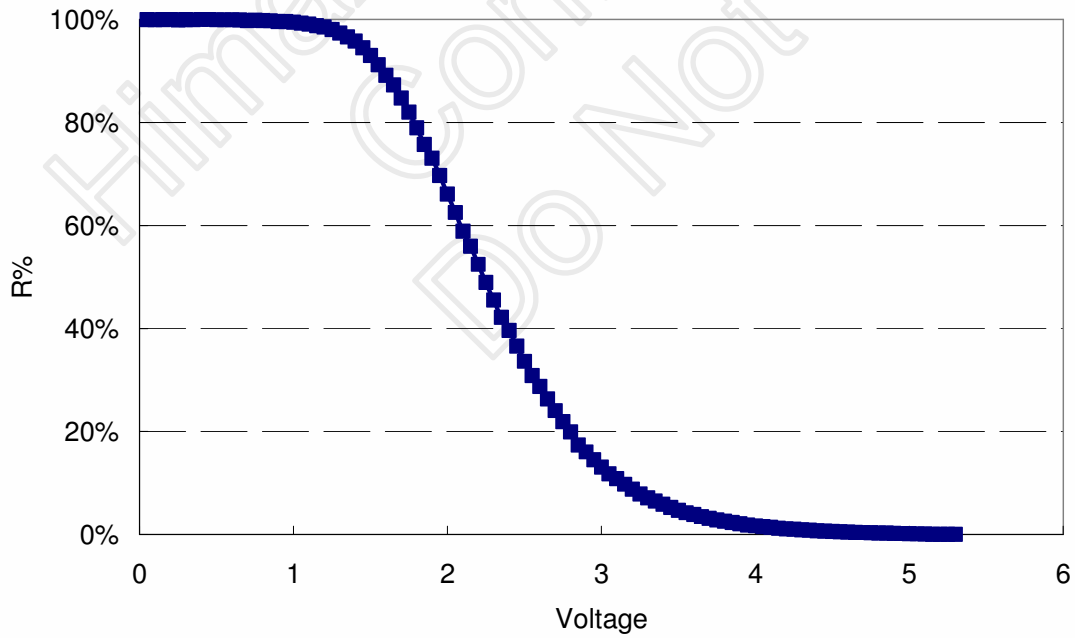
11.3 HX7027 Panel Reflection Spectrum

Reflection spectrum is measured by MDIS (Westar Inc.)



11.4 HX7027 Panel R-V Curves

The R-V Curve is measured by MDIS (Westar Inc.).



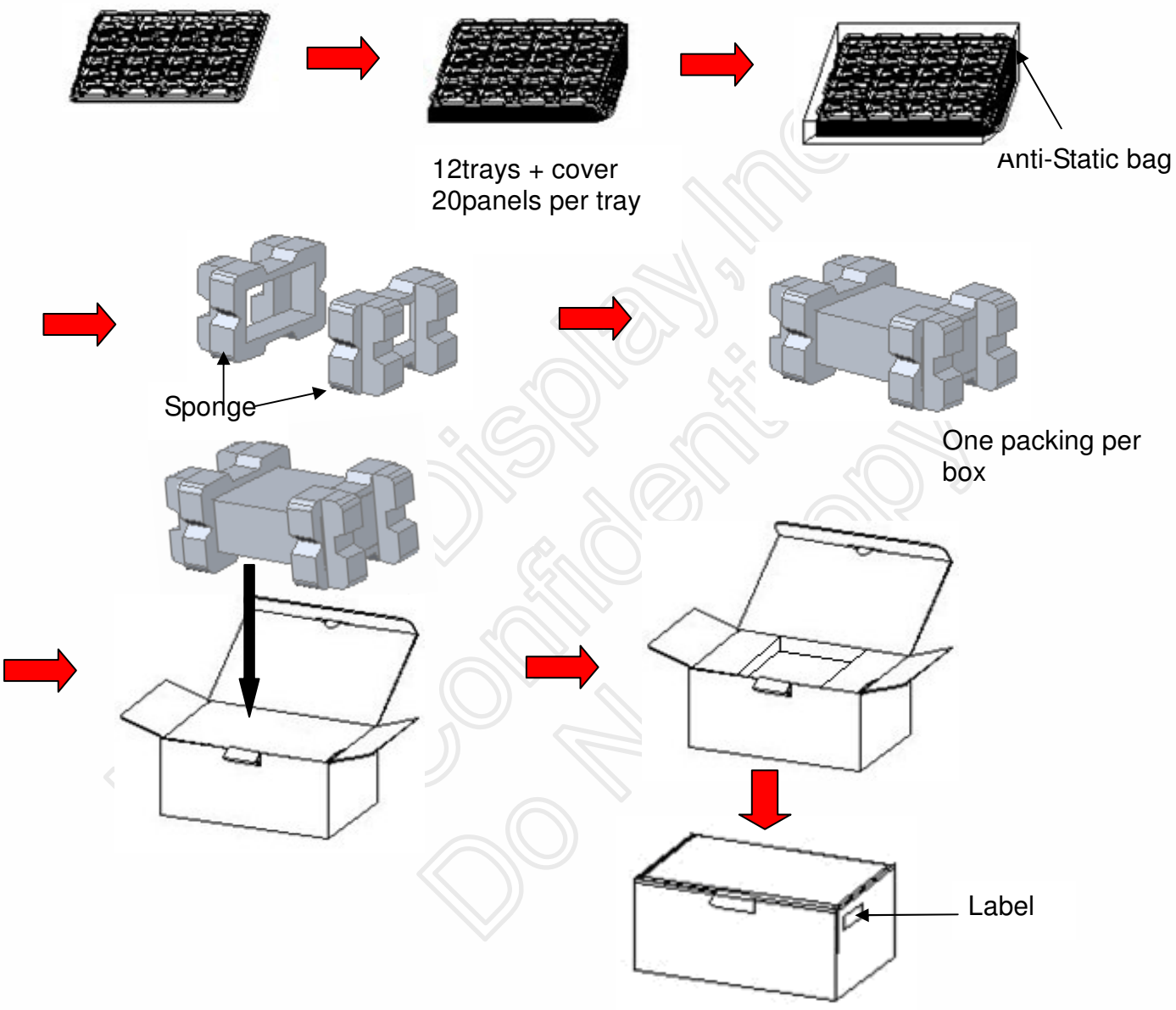
12. Reliability Test

Item	Specification	Judgment Criteria
HTST : High Temperature Storage Test	85 ºC , 240 hrs , 3 pcs	After being returned to the normal temperature and being left for more than 2 hours , the judgment is made according to Note A、B、C、D
LTST : Low Temperature Storage Test	-40ºC , 240 hrs , 3 pcs	
HTHHST : High Temperature and High Humidity Storage Test	60 ºC , 90%RH , 240 hrs, 3 pcs	
TCST : Temperature Cycling Storage Test	-20 ºC (0.5 hr) / 60ºC (0.5 hr), 100 cycles, 3 pcs	
HTBT : High Temperature Bias Test	70 ºC , 240 hrs, 3 pcs	
HTHHBT High Temperature and High Humidity Bias Test	50 ºC, 90%RH , 240 hrs, 3 pcs	
LTBT : Low Temperature Bias Test	-20 ºC, 240 hrs, 3 pcs	
ALT Altitude Test	193mbar(12,000m) ,72 hrs,3pcs	
CNTPIO Connector Plug In and Out	20 times	After test , the judgment is made according to Note B、C、D
FPCB FPC Bending Test	± 90 degree, 500gf , 10 times	
Package Vibration Proof	Follow ISTA Spec, 1 Box	
Package Drop Test	Follow ISTA Spec, 1 Box	
Note: A. CR after RA test is higher than one half of the initial CR. B. No functional failure. C. No extra mura or defect. D. No obvious deformation or break.		

13. Package Specifications

- Box content : 12 trays + cover tray. (Note: Each trays can contain 20 panels).
- Box dimension : 368 (L) x 175 (W) x 245 (H) (Unit: mm)
- Gross Weight : Approximately 1.9 kg

13.1 Packing Procedure



13.2 Label Information

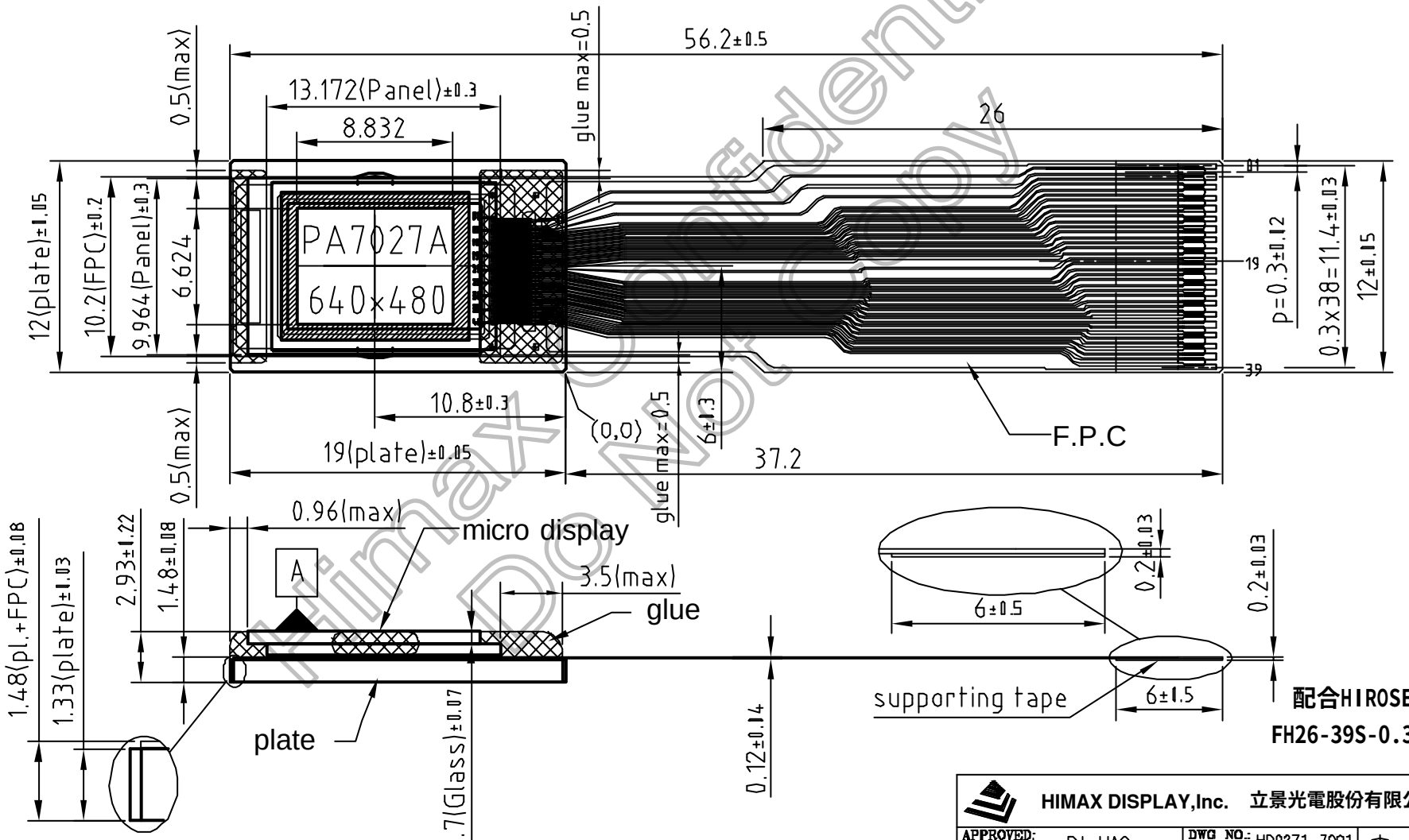
Label information indicate grading of LCOS module, part ID, module name and shipping quantity.

14. Green Product

HX7027ATGFA is a RoHS (Restriction on the use of certain Hazardous Substances) compliance product.

15. Mechanical Dimension

The mechanical dimensions are for customer’s reference design-in purpose. The mechanical dimensions has indicated as the drawing, HX7027-Module-01 as shown on the following page.



1.The UV glue should not approach the A side.

NOTE : If actual drawing has tolerance it will be based on actual drawing.

NO: 8-3088-0 6 Ver.0 2

MARK	DESCRIPTION	DATE	CHANGE BY	APPROVAL BY	ECN NO.
REV.04	Add Glass thickness dimension & tolerance	02/5/2008	Hannah_Chan	ALLEN_Wu	
REV.03	New definition for UV glue zone to protect Ag-glue	12/20/2007	ALLEN_WU	JERRY_SU	
Rev.02	Cancel "WORKING SAMPLE" text for MP	10/29/2007	Hannah_Chen	Tony_Tan	

RANGE	TOLERANCE

HIMAX DISPLAY,Inc. 立景光電股份有限公司

APPROVED: BJ_LIAO	DWG NO.: HD0271-7001				
CHECKED: JERRY_SU	DATE: 02/05/2008				
DESIGNER: ALLEN_WU	PART NO.:				
DRAWER: HANNAH_CHAN	REV.: 04	UNIT:	SCALE:	SHEET:	
TITLE: HX7027-MODULE-01		mm	1:1	SHEET	
PROJCET CODE: HD0000					