ARM® ARM926EJ-S Based
32-bit Microprocessor

N9H30 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

Table of Contents

LIST OF FIGURES

LIST OF TABLES

No table of figures entries found.

1 GENERAL DESCRIPTION

The N9H30 series targeted for general purpose 32-bit microcontroller embeds an outstanding CPU core ARM926EJ-S, runs up to 300 MHz, with 16 KB I-cache, 16 KB D-cache and MMU, 56KB embedded SRAM and 16 KB IBR (Internal Boot ROM) for booting from USB, NAND and SPI FLASH.

The N9H30 series integrates USB 2.0 HS HOST/Device controller with HS transceiver embedded, TFT type LCD controller, 2D graphics engine, I^2S I/F controller, SD/MMC/NAND FLASH controller, GDMA and 8 channels 12-bit ADC controller with resistance touch screen functionality. It also integrates UART, SPI/MICROWIRE, I^2C, LIN, PWM, Timer, WDT/Windowed-WDT, GPIO, Keypad, Smart Card I/F, 32.768 KHz XTL and RTC (Real Time Clock).

In addition, the N9H30 series integrates a DRAM I/F that runs up to 150MHz with supporting DDR or DDR2 type SDRAM. To reduce system complexity while cutting the BOM cost, the N9H30 series provides MCP (Multi-Chip Package) to ensure higher performance and to minimize the system design efforts.

2 FEATURES

1.1 Features

Core

- ARM® ARM926EJ-S™ processor core runs up to 300 MHz
- Support 16 KB instruction cache and 16 KB data cache
- Support MMU
- Support JTAG Debug interface

- DDR SDRAM Controller
  - Support LVDDR and DDR2 SDRAM
  - Clock speed up to 150 MHz
  - Support 16-bit data bus width
  - Memory size depended on embedded SDRAM configuration by different part number.
- Embedded SRAM and ROM
  - Support 56K bytes embedded SRAM
  - Support 16K bytes Internal Boot ROM (IBR)
  - Support up to four booting modes
  - Boot from USB
  - Boot from eMMC
  - Boot from NAND Flash
  - Boot from SPI Flash
- Clock Control
  - Support two PLLs, up to 500 MHz, for high performance system operation
  - External 12 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low speed clock source
- USB 2.0 Controller
  - Support USB Revision 2.0 specification
  - Support one set of USB 2.0 High-Speed (HS) Device/Host with embedded transceiver
  - Support one set of USB 2.0 High-Speed (HS) Host with embedded transceiver
  - Support Control, Bulk, Interrupt, Isochronous and Split transfers
  - Support USB host function compliant to Enhanced Host Controller Interface (EHCI) 1.0 specification to connect with USB 2.0 High-Speed (HS) device.
  - Support USB host function compliant to Open Host Controller Interface (OHCI) 1.0 specification to connect with USB 1.1 Full-Speed (FS) and Low-Speed (LS) devices
  - Support USB High-Speed (HS) and Full-Speed (FS) device function
  - Support USB device function with 1 endpoint for Control IN/OUT transfers and 12 programmable endpoints for Bulk, Interrupt and Isochronous IN/OUT transfers
  - Support suspend, resume and remote wake-up capability
  - Support DMA function
  - Support 2048 Bytes internal SRAM for USB host function and 4096 Bytes internal SRAM for USB device function
- Flash Memory Interface
  - Support NAND flash interface
  - Support 8-bit data bus width
  - Support SLC and MLC type NAND flash device
  - Support 512 B, 2 KB, 4 KB and 8 KB page size NAND flash device
  - Support ECC4, ECC8, ECC12, ECC15 and ECC24 BCH algorithm for ECC code generation, error detection and error correction.
  - Support eMMC flash interface
  - Support DMA function to accelerate the data transfer between system memory and

NAND and eMMC flash.

- I²S Controller
  - Support I²S interface
    - Support both mono and stereo
    - Support both record and playback
    - Support 8-bit, 16-bit 20-bit and 24-bit data precision
    - Support master and slave mode
  - Support PCM interface
    - Support 2 slots mode to connect 2 device
    - Support 8-bit, 16-bit 20-bit and 24-bit data precision
    - Support master mode
  - Support four 8x24 (8 24-bit) buffer for left/right channel record and left/right playback
  - Support DMA function to accelerate the data transfer between system memory and internal buffer
  - Support 2 buffer address for left/right channel and 2 slots data transfer
- LCD Display Controller
  - Support 8/9/16/18/24-bit data with to connect with 80/68 series MPU type LCD module
  - Support resolution up to 1024x768
  - Support data format conversion from RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 to RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 for display output
  - Support CCIR-656 (with VSYNC, HSYNC and data enable sync signal) 8/16-bit YUV data output to connect with external TV encoder
  - Support 8/16 bpp OSD data with video overlay function to facilitate the diverse graphic UI
  - Support linear 1X to 8X image scaling up function
  - Support Picture-In-Picture display function
  - Support hardware cursor
- 2D Graphic Engine
  - Support 2D Bit Block Transfer (BitBLT) functions defined in Microsoft GDI
  - Support Host BLT
  - Support Pattern BLT
  - Support Color/Font Expanding BLT
  - Support Transparent BLT
  - Support Tile BLT
  - Support Block Move BLT
  - Support Copy File BLT
  - Support Color/Font Expansion
  - Support Rectangle Fill
  - Support RGB332/RGB565/RGB888 data format.
  - Support fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
  - Support both inside and outside clipping function
  - Support alpha-blending for source/destination picture overlaying
  - Support fast Bresenham line drawing algorithm to draw solid/textured line
  - Support rectangular border and frame drawing
  - Support picture re-sizing
  - Support down-scaling from 1/255 to 254/255
  - Support up-scaling from 1 to 1.996 (1+254/255)
  - Support object rotation with different degree
  - Support L45 (45 degree left rotation) and L90 (90 degree left rotation)
  - Support R45 (45 degree right rotation) and R90 (90 degree right rotation)
  - Support M180 (mirror/flop)
  - Support F180 (up-side-down (flip) and X180 (180 degree rotation)

- JPEG Codec
  - Support Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard
  - Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
  - Support rotate function in encode mode
  - Packet Format
  - Support to encode interleaved YUYV format input image, output bit stream 4:2:2 and 4:2:0 format
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
  - Support decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
- GDMA (General DMA)
  - Support 2 channels GDMA for memory-to-memory data transfer without CPU intervention
  - Support increment and decrement for source and destination address calculation
  - Support 8-bit, 16-bit and 32-bit width data transfer
  - Support four 8-bit/16-bit/32-bit burst transfer
- UART
  - Support up to 11 UART controllers
  - Support 1 UART (UART 1) port with full model function (TXD, RXD, CTS, RTS, CDn, RIn, DTR and DSR) and 64-byte FIFO
  - Support 5 UART (UART 2/4/6/8/10) ports with flow control (TXD, RXD, CTS and RTS) and 64-byte FIFO
  - Support 5 TXD/RXD only UART ports (UART 0/3/5/7/9) with 16-byte FIFO for standard device
  - Support IrDA (SIR) and LIN function
  - Support RS-485 9-bit mode and direction control
  - Support programmable baud-rate generator up to 1/16 system clock
- Smart Card Host (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level

- Programmable guard time selection (11 ETU ~ 266 ETU)
- One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error limit function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detecting the card removal

- Timer
  - Support 5 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Support one-shot, periodic, toggle and continuous operation modes
- Enhanced Timer
  - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Support one-shot, periodic, toggle and continuous operation modes
  - Supports external pin capture for interval measurement
  - Supports external pin capture for timer counter reset
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.333us ~ 14.316sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable on watchdog timer time-out
- Windowed-Watchdog Timer
  - 6-bit down counter with 11-bit pre-scale for wide range window selected
  - Interrupt on windowed-watchdog timer time-out
  - Reset on windowed-watchdog timer time out or reload in an unexpected time window
- Real Time Clock (RTC)
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (VBAT)
- PWM
  - Built-in up to two 16-bit PWM generators provide four PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit pre-scale, two 16-bit counters, and one Dead-Zone generator
- SPI
  - Built-in up to two sets of SPI controller
  - Support SPI master mode
  - Support single/dual/quad bit data bus width
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Support burst mode operation that transmission and reception can be executed up to four times in a transfer

- I^2C
  - Up to two sets of I^2C device
  - Support master mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support software mode to generate I^2C signaling
- Advanced Interrupt Controller
  - Support 58 interrupt sources, including 8 external interrupt sources
  - Support programmable normal or fast interrupt mode (IRQ, FIQ)
  - Support programmable edge-triggered or level-sensitive for 8 external interrupt sources
  - Support programmable low-active or high-active for 8 external interrupt sources
  - Support encoded priority methodology to allow for interrupt daisy-chaining
  - Support lower priority interrupt automatically mask out for nested interrupt
  - Support to clear interrupt flag automatically if interrupt source is programmed as edge-triggered
- GPIO
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Support pull-up and pull-down control
- ADC
  - 12-bit SAR ADC with 800K/160K SPS
  - Up to 5-ch single-end input
  - Support up to 800K SPS in channel 1 and up to 160K SPS in others channels.
  - Support 4-wire or 5-wire resistance touch screen interface
  - Support touch pressure measurement for 4-wire touch screen application
  - Support pen down detection
- MTP
  - Support 256-bit programmable memory
  - Support up to 15 times of programming and erase.
- Low Voltage Detect (LVD) and Low Voltage Reset (LVR)
  - Support two, 2.6V and 2.8V, voltage detection levels
  - Interrupt when low voltage detected
  - Reset when low voltage detected
  - Low voltage reset threshold voltage levels: 2.4 V
- Power Management
  - Advanced power management including Power Down, Deep Standby, CPU Standby and Normal Operating modes
  - Normal Operating mode
    - CPU run normally and all clocks on, the current consumption of CORE_VDD is around 185 mA (at CPU/DRAM clock is 300/150 MHz CPU).
  - CPU Standby mode
    - CPU clock stop, and all other clocks on.
  - Deep Standby mode

        - All clocks stop, except LXT, with SRAM retention, and the current consumption of CORE_VDD is typicaly 3 mA
    - Power Down mode
        - All powers are off except RTC_VDD (3.3V) and the current consumption of RTC_VDD is typicaly 7uA with RTC functionality on.
- Operating Voltage
    - 1.2V for core logic operating
    - 1.8V for DDR or DDR2 SDRAM I/O operating
    - 3.3V for normal I/O operating
- Operating Temperature: -40℃~85℃
- Packages:
    - All Green package (RoHS)
    - LQFP 216-pin
    - LQFP 128-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 N9H30 Series Part Number Naming Guide

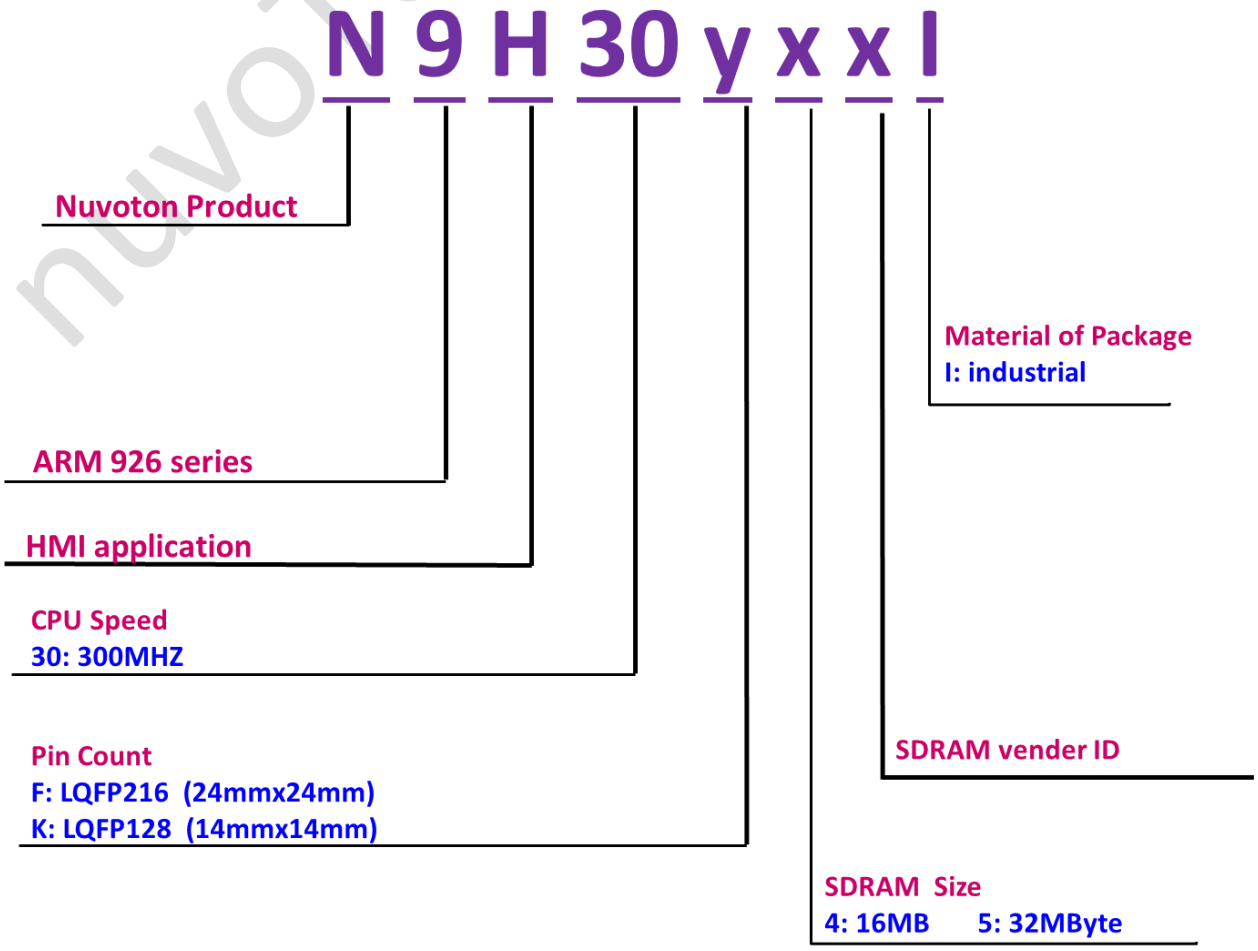


Figure 3-1 N9H30 Series Part Number Naming Guide

3.2 N9H30 Series Part Selection Guide

N9H30 series

Part No.	Memory		Storage			MAC	USB		GFX	LCD	Timer						Analog				Peripheral										Package	Operating Temp. Range1 (°C)
																	ADC															
	DDR2 RAM(MB)	SPI Flash, No. of I/O Pins	NAND Flash, No. of ECC bits	EMMC	SD / SDIO	Ethernet 10/100 MAC	USB 2.0 Host (480M bps)	USB 2.0 HS Device	2D Graphics	TFT LCD	Real-Time Clock (RTC)	Timer (32-bit)	Enhanced Timer Measurement	Watchdog Timer	Window Watchdog Timer	PWM	Touch Screen Controller	No. of Channels	Speed (Samples per second)	LVD/LVR	External Bus Interface	GPIO (Max)	UART	CAN BUS	I2C (Master Only)	SPI	ISO-7816-3	KPI	CMOS Interface	I²S		
N9H30F51I	32	1	24	√	2	2	2	1	√	24-bit	√	5	4	√	√	4	√	8	200K*	√	√	146	11	-	2	2	2	-	-	1	LQFP216	-40 to +85
N9H30K41I	16	1	24	√	2	-	2	1	√	16-bit	√	5	1	√	√	4	√	5	200K*	√	-	86	9	-	2	2	2	-	-	1	LQFP128	-40 to +85

3.3 Pin Configuration

3.3.1 N9H30KxxI Series Pin Diagram

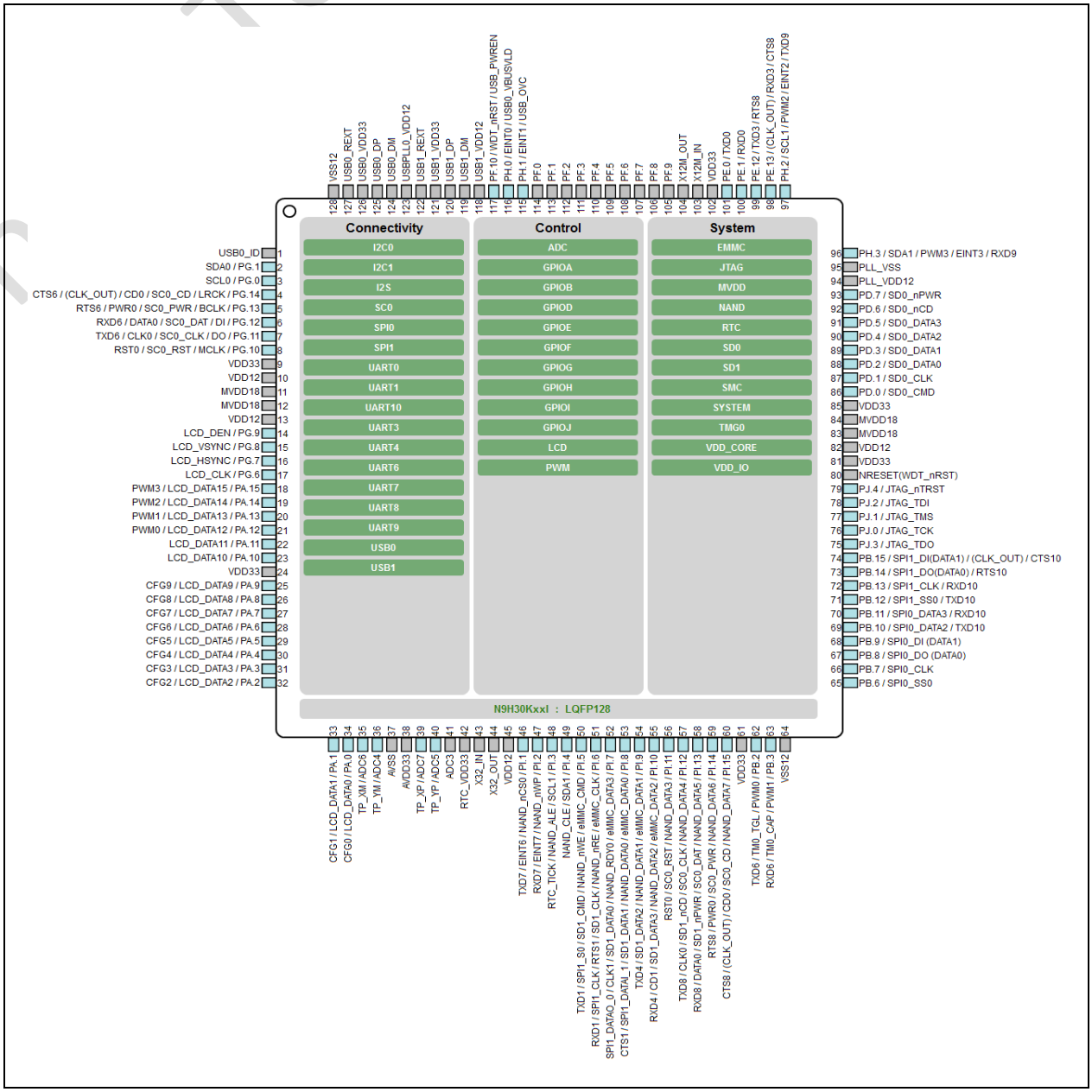


Figure 3.3-1 N9H30KxxI Series LQFP 128-pin Pin Diagram

3.3.2 N9H30FxxI Series Pin Diagram

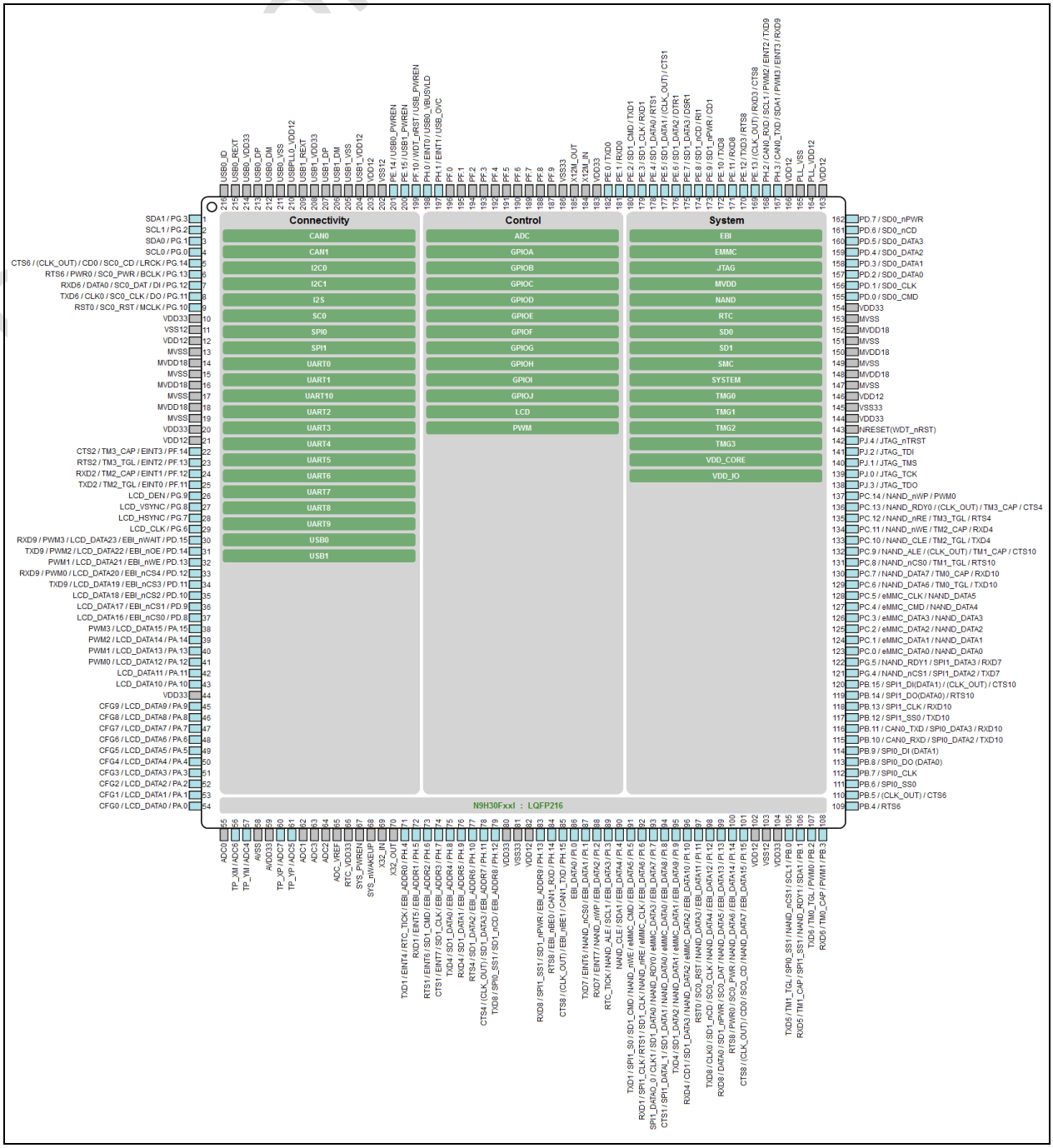


Figure 3.3-2 N9H30FxxI Series LQFP 216-pin Pin Diagram

4 PIN DESCRIPTION

4.1.1 N9H30KxxI LQFP128 Pin List

N9H30KxxI	Pin Name	Pin Type	Description
1	USB0_ID	IU	USB0 Host/Device select.
2	PG.1	I/O	General purpose digital I/O pin Port G Pin 1.
	I2C0_SDA	I/O	I^2C0 data input/output pin.
3	PG.0	I/O	General purpose digital I/O pin Port G Pin 0.
	I2C0_SCL	O	I^2C0 clock pin.
4	PG.14	I/O	General purpose digital I/O pin Port G Pin 14.
	I2S_LRCK	O	I^2S left right channel clock.
	UART6_CTS	I	Clear to send input pin for UART6.
	SC0_CD	I	SmartCard0 card detect pin.
	CLK_OUT	O	Reference Clock Output.
5	PG.13	I/O	General purpose digital I/O pin Port G Pin 13.
	I2S_BCLK	I	I^2S bit clock pin.
	UART6_RTS	O	Request to send output pin for UART6.
	SC0_PWR	O	SmartCard0 power pin.
6	PG.12	I/O	General purpose digital I/O pin Port G Pin 12.
	I2S_DI	I	I^2S data input.
	UART6_RXD	I	Data receiver input pin for UART6.
	SC0_DAT	I/O	SmartCard0 data pin.
7	PG.11	I/O	General purpose digital I/O pin Port G Pin 11.
	I2S_DO	O	I^2S data output.
	UART6_TXD	O	Data transmitter output pin for UART6.
	SC0_CLK	O	SmartCard0 clock pin.
8	PG.10	I/O	General purpose digital I/O pin Port G Pin 10.
	I2S_MCLK	O	I^2S master clock output pin.
	SC0_RST	O	SmartCard0 reset pin.
9	IO_VDD	P	MCU I/O power pin.
10	CORE_VDD	P	MCU internal core power pin.
11	DDR_VDD	P	DDR power pin.
12	DDR_VDD	P	DDR power pin.
13	CORE_VDD	P	MCU internal core power pin.
14	PG.9	I/O	General purpose digital I/O pin Port G Pin 9.

	LCD_DEN	O	Data enable or display control signal.
15	PG.8	I/O	General purpose digital I/O pin Port G Pin 8.
	LCD_VSYNC	O	Vertical sync or frame sync.
16	PG.7	I/O	General purpose digital I/O pin Port G Pin 7.
	LCD_HSYNC	O	Horizontal sync or line sync.
17	PG.6	I/O	General purpose digital I/O pin Port G Pin 6.
	LCD_CLK	O	Pixel clock output.
18	PA.15	I/O	General purpose digital I/O pin Port A Pin 15.
	LCD_DATA15	O	LCD pixel data output bit 15.
	PWM3	O	PWM3 output pin.
19	PA.14	I/O	General purpose digital I/O pin Port A Pin 14.
	LCD_DATA14	O	LCD pixel data output bit 14.
	PWM2	O	PWM2 output pin.
20	PA.13	I/O	General purpose digital I/O pin Port A Pin 13.
	LCD_DATA13	O	LCD pixel data output bit 13.
	PWM1	O	PWM1 output pin.
21	PA.12	I/O	General purpose digital I/O pin Port A Pin 12.
	LCD_DATA12	O	LCD pixel data output bit 12.
	PWM0	O	PWM0 output pin.
22	PA.11	I/O	General purpose digital I/O pin Port A Pin 11.
	LCD_DATA11	O	LCD pixel data output bit 11.
23	PA.10	I/O	General purpose digital I/O pin Port A Pin 10.
	LCD_DATA10	O	LCD pixel data output bit 10.
24	IO_VDD	P	MCU I/O power pin.
25	PA.9	I/O	General purpose digital I/O pin Port A Pin 9.
	LCD_DATA9	O	LCD pixel data output bit 9.
	PWRON_SET9	IU	Power On Setting bit 9.
26	PA.8	I/O	General purpose digital I/O pin Port A Pin 8.
	LCD_DATA8	O	LCD pixel data output bit 8.
	PWRON_SET8	IU	Power On Setting bit 8.
27	PA.7	I/O	General purpose digital I/O pin Port A Pin 7.
	LCD_DATA7	O	LCD pixel data output bit 7.
	PWRON_SET7	IU	Power On Setting bit 7.
28	PA.6	I/O	General purpose digital I/O pin Port A Pin 6.
	LCD_DATA6	O	LCD pixel data output bit 6.
	PWRON_SET6	IU	Power On Setting bit 6.
29	PA.5	I/O	General purpose digital I/O pin Port A Pin 5.

	LCD_DATA5	O	LCD pixel data output bit 5.
	PWRON_SET5	IU	Power On Setting bit 5.
30	PA.4	I/O	General purpose digital I/O pin Port A Pin 4.
	LCD_DATA4	O	LCD pixel data output bit 4.
	PWRON_SET4	IU	Power On Setting bit 4.
31	PA.3	I/O	General purpose digital I/O pin Port A Pin 3.
	LCD_DATA3	O	LCD pixel data output bit 3.
	PWRON_SET3	IU	Power On Setting bit 3.
32	PA.2	I/O	General purpose digital I/O pin Port A Pin 2.
	LCD_DATA2	O	LCD pixel data output bit 2.
	PWRON_SET2	IU	Power On Setting bit 2.
33	PA.1	I/O	General purpose digital I/O pin Port A Pin 1.
	LCD_DATA1	O	LCD pixel data output bit 1.
	PWRON_SET1	IU	Power On Setting bit 1.
34	PA.0	I/O	General purpose digital I/O pin Port A Pin 0.
	LCD_DATA0	O	LCD pixel data output bit 0.
	PWRON_SET0	IU	Power On Setting bit 0.
35	ADC0	I	ADC input channel 0 or VBAT.
36	ADC6	I	ADC input channel 6 or XM.
37	AVSS	P	Ground pin for analog circuit.
38	AVDD	P	Power supply for internal analog circuit.
39	ADC7	I	ADC input channel 7 or XP.
40	ADC5	I	ADC input channel 5 or YP.
41	ADC3	I	ADC input channel 3 or VSENSE.
42	RTC_VDD	P	RTC power input. (*. or 3.3V)
43	X32_IN	I	External 32.768kHz crystal input.
44	X32_OUT	O	External 32.768kHz crystal output.
45	CORE_VDD	P	MCU internal core power pin.
46	PI.1	I/O	General purpose digital I/O pin Port I Pin 1.
	NAND_nCS0	O	NAND flash chip select 0.
	UART7_TXD	O	Data transmitter output pin for UART7.
	INT6	I	External interrupt 6 input pin.
47	PI.2	I/O	General purpose digital I/O pin Port I Pin 2.
	NAND_nWP	O	NAND flash srite protect.
	UART7_RXD	I	Data receiver input pin for UART7.
	INT7	I	External interrupt 7 input pin.
48	PI.3	I/O	General purpose digital I/O pin Port I Pin 3.

	NAND_ALE	O	NAND flash address latch enable.
	I2C1_SCL	O	I^2C1 clock pin.
	RTC_TICK	O	RTC tick output
49	PI.4	I/O	General purpose digital I/O pin Port I Pin 4.
	NAND_CLE	O	NAND flash command latch enable.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
50	PI.5	I/O	General purpose digital I/O pin Port I Pin 5.
	NAND_nWE	O	NAND flash write enable.
	eMMC_CMD	I/O	eMMC command/Response.
	SD1_CMD	O	SD/SDIO mode #1 – command/response.
	UART1_TXD	O	Data transmitter output pin for UART1.
	SPI1_SS0	O	1st SPI1 chip select pin.
51	PI.6	I/O	General purpose digital I/O pin Port I Pin 6.
	NAND_nRE	O	NAND flash read enable.
	eMMC_CLK	O	eMMC clock output.
	SC1_RST	O	SmartCard1 reset pin.
	SD1_CLK	O	SD/SDIO mode #1– clock.
	UART1_RXD	I	Data receiver input pin for UART1.
	SPI1_CLK	O	SPI1 serial clock pin.
52	PI.7	I/O	General purpose digital I/O pin Port I Pin 7.
	NAND_RDY0	I	NAND flash ready/busy channel 0.
	eMMC_DATA3	I/O	eMMC data line bit 3.
	SC1_CLK	O	SmartCard1 clock pin.
	SD1_DAT0	I/O	SD/SDIO mode #1 data line bit 0.
	UART1_RTS	O	Request to send output pin for UART1.
	SPI1_DO (SPI1_DATA0)	I (I/O)	SPI1 Data out pin. (SPI1 data 0 in dual/quad mode.)
53	PI.8	I/O	General purpose digital I/O pin Port I Pin 8.
	NAND_DATA0	I/O	NAND flash data bus bit 0.
	eMMC_DATA0	I/O	eMMC data line bit 0.
	SC1_DAT	I/O	SmartCard1 data pin.
	SD1_DAT1	I/O	SD/SDIO mode #1 data line bit 1.
	UART1_CTS	I	Clear to send input pin for UART1.
	SPI1_DI (SPI1_DATA1)	I (I/O)	SPI1 Data input pin. (SPI1 data 1 in dual/quad mode.)
54	PI.9	I/O	General purpose digital I/O pin Port I Pin 9.
	NAND_DATA1	I/O	NAND flash data bus bit 1.

	eMMC_DATA1	I/O	eMMC data line bit 1.
	SC1_PWR	O	SmartCard1 power pin.
	SD1_DAT2	I/O	SD/SDIO mode #1 data line bit 2.
	UART4_TXD	O	Data transmitter output pin for UART4.
55	PI.10	I/O	General purpose digital I/O pin Port I Pin 10.
	NAND_DATA2	I/O	NAND flash data bus bit 2.
	eMMC_DATA2	I/O	eMMC data line bit 2.
	SC1_CD	I	SmartCard1 card detect pin.
	SD1_DAT3	I/O	SD/SDIO mode #1 data line bit 3.
	UART4_RXD	I	Data receiver input pin for UART4.
56	PI.11	I/O	General purpose digital I/O pin Port I Pin 11.
	NAND_DATA3	I/O	NAND flash data bus bit 3.
	SC0_RST	O	SmartCard0 reset pin.
57	PI.12	I/O	General purpose digital I/O pin Port I Pin 12.
	NAND_DATA4	I/O	NAND flash data bus bit 4.
	UART8_TXD	O	Data transmitter output pin for UART8.
	SC0_CLK	O	SmartCard0 clock pin.
	SD1_nCD	I	SD/SDIO mode #1 – card detect.
58	PI.13	I/O	General purpose digital I/O pin Port I Pin 13.
	NAND_DATA5	I/O	NAND flash data bus bit 5.
	UART8_RXD	I	Data receiver input pin for UART8.
	SC0_DAT	I/O	SmartCard0 data pin.
	SD1_nPWR	O	SD/SDIO mode #1 – power enable.
59	PI.14	I/O	General purpose digital I/O pin Port I Pin 14.
	NAND_DATA6	I/O	NAND flash data bus bit 6.
	UART8_RTS	O	Request to send output pin for UART8.
	SC0_PWR	O	SmartCard0 power pin.
60	PI.15	I/O	General purpose digital I/O pin Port I Pin 15.
	NAND_DATA7	I/O	NAND flash data bus bit 7.
	UART8_CTS	I	Clear to send input pin for UART8.
	SC0_CD	I	SmartCard0 card detect pin.
	CLK_OUT	O	Clock output pin.
61	IO_VDD	P	MCU I/O power pin.
62	PB.2	I/O	General purpose digital I/O pin Port B Pin 2.
	UART6_TXD	O	Data transmitter output pin for UART6.
	PWM0	O	PWM0 output pin.
	TM0_TGL	O	Enhanced TIMER toggle output pin.

63	PB.3	I/O	General purpose digital I/O pin Port B Pin 3.
	UART6_RXD	I	Data receiver input pin for UART6.
	PWM1	O	PWM1 output pin.
	TM0_CAP	I	Enhanced TIMER capture input pin.
64	GND	P	Ground pin for digital.
65	PB.6	I/O	General purpose digital I/O pin Port B Pin 6.
	SPI0_SS0	O	1st SPI0 chip select pin.
66	PB.7	I/O	General purpose digital I/O pin Port B Pin 7.
	SPI0_CLK	O	SPI0 serial clock pin.
67	PB.8	I/O	General purpose digital I/O pin Port B Pin 8.
	SPI0_DO (SPI0_DATA0)	O (I/O)	SPI0 Data out pin. (SPI0 data 0 in dual/quad mode.)
68	PB.9	I/O	General purpose digital I/O pin Port B Pin 9.
	SPI0_DI (SPI0_DATA1)	I (I/O)	SPI0 Data input pin. (SPI0 data 1 in dual/quad mode.)
69	PB.10	I/O	General purpose digital I/O pin Port B Pin 10.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI0_DATA2	I/O	SPI0 data 2 in dual/quad mode.
70	PB.11	I/O	General purpose digital I/O pin Port B Pin 11.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI0_DATA3	I/O	SPI0 data 3 in dual/quad mode.
71	PB.12	I/O	General purpose digital I/O pin Port B Pin 12.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI1_SS0	O	1st SPI1 chip select pin.
72	PB.13	I/O	General purpose digital I/O pin Port B Pin 13.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI1_CLK	O	SPI1 serial clock pin.
73	PB.14	I/O	General purpose digital I/O pin Port B Pin 14.
	UART10_RTS	O	Request to send output pin for UART10.
	SPI1_DO (SPI1_DATA0)	O (I/O)	SPI1 Data out pin. (SPI1 data 0 in dual/quad mode.)
74	PB.15	I/O	General purpose digital I/O pin Port B Pin 15.
	UART10_CTS	I	Clear to send input pin for UART10.
	SPI1_DI (SPI1_DATA1)	I (I/O)	SPI1 Data input pin. (SPI1 data 1 in dual/quad mode.)
75	PJ.3	I/O	General purpose digital I/O pin Port J Pin 3.
	JTAG_TDO	O	JTAG test data out.

76	PJ.0	I/O	General purpose digital I/O pin Port J Pin 0.
	JTAG_TCK	O	JTAG test clock.
77	PJ.1	I/O	General purpose digital I/O pin Port J Pin 1.
	JTAG_TMS	O	JTAG test mode select.
78	PJ.2	I/O	General purpose digital I/O pin Port J Pin 2.
	JTAG_TDI	I	JTAG test data in.
79	PJ.4	I/O	General purpose digital I/O pin Port J Pin 4.
	JTAG_nTRST	O	JTAG Reset.
80	nRESET	IU	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
	WDT_nRST	O	Watch dog timer external reset output pin. Open-drain.
81	IO_VDD	P	MCU I/O power pin.
82	CORE_VDD	P	MCU internal core power pin.
83	DDR_VDD	P	DDR power pin.
84	DDR_VDD	P	DDR power pin.
85	IO_VDD	P	MCU I/O power pin.
86	PD.0	I/O	General purpose digital I/O pin Port D Pin 0.
	SD0_CMD	O	SD/SDIO mode #0 command/response.
87	PD.1	I/O	General purpose digital I/O pin Port D Pin 1.
	SD0_CLK	O	SD/SDIO mode #0 clock.
88	PD.2	I/O	General purpose digital I/O pin Port D Pin 2.
	SD0_DAT0	I/O	SD/SDIO mode #0 data line bit 0.
89	PD.3	I/O	General purpose digital I/O pin Port D Pin 3.
	SD0_DAT1	I/O	SD/SDIO mode #0 data line bit 1.
90	PD.4	I/O	General purpose digital I/O pin Port D Pin 4.
	SD0_DAT2	I/O	SD/SDIO mode #0 data line bit 2.
91	PD.5	I/O	General purpose digital I/O pin Port D Pin 5.
	SD0_DAT3	I/O	SD/SDIO mode #0 data line bit 3.
92	PD.6	I/O	General purpose digital I/O pin Port D Pin 6.
	SD0_nCD	I	SD/SDIO mode #0 card detect.
93	PD.7	I/O	General purpose digital I/O pin Port D Pin 7.
94	PLL_VDD	P	PLL power input pin.
95	PLL_VSS	P	PLL ground.
96	PH.3	I/O	General purpose digital I/O pin Port H Pin 3.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM3	O	PWM3 output pin.
	INT3	I	External interrupt 3 input pin.

97	PH.2	I/O	General purpose digital I/O pin Port H Pin 2.
	I2C1_SCL	O	I^2C1 clock pin.
	UART9_TXD	O	Data transmitter output pin for UART9.
	PWM2	O	PWM2 output pin.
	INT2	I	External interrupt 2 input pin.
98	PE.13	I/O	General purpose digital I/O pin Port E Pin 13.
	UART8_CTS	I	Clear to send input pin for UART8.
	UART3_RXD	I	Data receiver input pin for UART3.
	CLK_OUT	O	Reference Clock Output.
99	PE.12	I/O	General purpose digital I/O pin Port E Pin 12.
	UART8_RTS	O	Request to send output pin for UART8.
	UART3_TXD	O	Data transmitter output pin for UART3.
100	PE.1	I/O	General purpose digital I/O pin Port E Pin 1.
	UART0_RXD	I	Data receiver input pin for UART0.
101	PE.0	I/O	General purpose digital I/O pin Port E Pin 0.
	UART0_TXD	O	Data transmitter output pin for UART0.
102	IO_VDD	P	MCU I/O power pin.
103	XT1_IN	I	External 12MHz crystal input pin.
104	XT1_OUT	O	External 12MHz crystal output pin.
105	PF.9	I/O	General purpose digital I/O pin Port F Pin 9.
106	PF.8	I/O	General purpose digital I/O pin Port F Pin 8.
107	PF.7	I/O	General purpose digital I/O pin Port F Pin 7.
108	PF.6	I/O	General purpose digital I/O pin Port F Pin 6.
109	PF.5	I/O	General purpose digital I/O pin Port F Pin 5.
110	PF.4	I/O	General purpose digital I/O pin Port F Pin 4.
111	PF.3	I/O	General purpose digital I/O pin Port F Pin 3.
112	PF.2	I/O	General purpose digital I/O pin Port F Pin 2.
113	PF.1	I/O	General purpose digital I/O pin Port F Pin 1.
114	PF.0	I/O	General purpose digital I/O pin Port F Pin 0.
115	PH.1	I/O	General purpose digital I/O pin Port H Pin 1.
	USB_OVRCUR	I	USB overcurrent
	INT1	I	External interrupt 1 input pin.
116	PH.0	I/O	General purpose digital I/O pin Port H Pin 0.
	USB0_VBUSVLD	I	USB0 VBUS valid.
	INT0	I	External interrupt 0 input pin.
117	PF.10	I/O	General purpose digital I/O pin Port F Pin 10.
	USB_PWREN	O	USB host output power control pin for LQFP128 package only.

118	USBPLL1_VDD	P	USB1 PLL power pin.
119	USB1_DM	I/O	USB1 differential signal D-.
120	USB1_DP	I/O	USB1 differential signal D+.
121	USB1_VDD	P	USB1 I/O power pin.
122	USB1_REXT	I	USB1 module reference Resister.
123	USBPLL0_VDD	P	USB0 PLL power pin.
124	USB0_DM	I/O	USB0 differential signal D-.
125	USB0_DP	I/O	USB0 differential signal D+.
126	USB0_VDD	P	USB0 I/O power pin.
127	USB0_REXT	I	USB0 module reference Resister.
128	GND	P	Ground pin for digital.

4.1.2 N9H30FxxI LQFP216 Pin List

N9H30FxxI	Pin Name	Pin Type	Description
1	PG.3	I/O	General purpose digital I/O pin Port G Pin 3.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
2	PG.2	I/O	General purpose digital I/O pin Port G Pin 2.
	I2C1_SCL	O	I^2C1 clock pin.
3	PG.1	I/O	General purpose digital I/O pin Port G Pin 1.
	I2C0_SDA	I/O	I^2C0 data input/output pin.
4	PG.0	I/O	General purpose digital I/O pin Port G Pin 0.
	I2C0_SCL	O	I^2C0 clock pin.
5	PG.14	I/O	General purpose digital I/O pin Port G Pin 14.
	I2S_LRCK	O	I^2S left right channel clock.
	UART6_CTS	I	Clear to send input pin for UART6.
	SC0_CD	I	SmartCard0 card detect pin.
	CLK_OUT	O	Reference Clock Output.
6	PG.13	I/O	General purpose digital I/O pin Port G Pin 13.
	I2S_BCLK	I	I^2S bit clock pin.
	UART6_RTS	O	Request to send output pin for UART6.
	SC0_PWR	O	SmartCard0 power pin.
7	PG.12	I/O	General purpose digital I/O pin Port G Pin 12.
	I2S_DI	I	I^2S data input.
	UART6_RXD	I	Data receiver input pin for UART6.
	SC0_DAT	I/O	SmartCard0 data pin.
8	PG.11	I/O	General purpose digital I/O pin Port G Pin 11.
	I2S_DO	O	I^2S data output.
	UART6_TXD	O	Data transmitter output pin for UART6.
	SC0_CLK	O	SmartCard0 clock pin.
9	PG.10	I/O	General purpose digital I/O pin Port G Pin 10.
	I2S_MCLK	O	I^2S master clock output pin.
	SC0_RST	O	SmartCard0 reset pin.

10	IO_VDD	P	MCU I/O power pin.
11	CORE_VSS	P	MCU internal core ground pin.
12	CORE_VDD	P	MCU internal core power pin.
13	DDR_VSS	P	DDR ground pin.
14	DDR_VDD	P	DDR power pin.
15	DDR_VSS	P	DDR ground pin.
16	DDR_VDD	P	DDR power pin.
17	DDR_VSS	P	DDR ground pin.
18	DDR_VDD	P	DDR power pin.
19	CORE_VSS	P	MCU internal core ground pin.
20	IO_VDD	P	MCU I/O power pin.
21	CORE_VDD	P	MCU internal core power pin.
22	PF.14	I/O	General purpose digital I/O pin Port F Pin 14.
	UART2_CTS	I	Clear to send input pin for UART2.
	TM3_CAP	I	Enhanced TIMER capture input pin.
	INT3	I	External interrupt 3 input pin.
23	PF.13	I/O	General purpose digital I/O pin Port F Pin 13.
	UART2_RTS	O	Request to send output pin for UART2.
	TM3_TGL	O	Enhanced TIMER toggle output pin.
	INT2	I	External interrupt 2 input pin.
24	PF.12	I/O	General purpose digital I/O pin Port F Pin 12.
	UART2_RXD	I	Data receiver input pin for UART2.
	TM2_CAP	I	Enhanced TIMER capture input pin.
	INT1	I	External interrupt 1 input pin.
25	PF.11	I/O	General purpose digital I/O pin Port F Pin 11.
	UART2_TXD	O	Data transmitter output pin for UART2.
	TM2_TGL	O	Enhanced TIMER toggle output pin.
	INT0	I	External interrupt 0 input pin.
26	PG.9	I/O	General purpose digital I/O pin Port G Pin 9.
	LCD_DEN	O	Data enable or display control signal.
27	PG.8	I/O	General purpose digital I/O pin Port G Pin 8.

	LCD_VSYNC	O	Vertical sync or frame sync.
28	PG.7	I/O	General purpose digital I/O pin Port G Pin 7.
	LCD_HSYNC	O	Horizontal sync or line sync.
29	PG.6	I/O	General purpose digital I/O pin Port G Pin 6.
	LCD_CLK	O	Pixel clock output.
30	PD.15	I/O	General purpose digital I/O pin Port D Pin 15.
	LCD_DATA23	O	LCD pixel data output bit 23.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM3	O	PWM3 output pin.
	EBI_nWAIT	I	External I/O wait control.
31	PD.14	I/O	General purpose digital I/O pin Port D Pin 14.
	LCD_DATA22	O	LCD pixel data output bit 22.
	UART9_TXD	O	Data transmitter output pin for UART9.
	PWM2	O	PWM2 output pin.
	EBI_nOE	O	External I/O output enable.
32	PD.13	I/O	General purpose digital I/O pin Port D Pin 13.
	LCD_DATA21	O	LCD pixel data output bit 21.
	PWM1	O	PWM1 output pin.
	EBI_nWE	O	External I/O chip write enable.
33	PD.12	I/O	General purpose digital I/O pin Port D Pin 12.
	LCD_DATA20	O	LCD pixel data output bit 20.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM0	O	PWM0 output pin.
	EBI_nCS4	O	External I/O chip select bank 4.
34	PD.11	I/O	General purpose digital I/O pin Port D Pin 11.
	LCD_DATA19	O	LCD pixel data output bit 19.
	UART9_TXD	O	Data transmitter output pin for UART9.
	EBI_nCS3	O	External I/O chip select bank 3.
35	PD.10	I/O	General purpose digital I/O pin Port D Pin 10.
	LCD_DATA18	O	LCD pixel data output bit 18.
	EBI_nCS2	O	External I/O chip select bank 2.

36	PD.9	I/O	General purpose digital I/O pin Port D Pin 9.
	LCD_DATA17	O	LCD pixel data output bit 17.
	EBI_nCS1	O	External I/O chip select bank 1.
37	PD.8	I/O	General purpose digital I/O pin Port D Pin 8.
	LCD_DATA16	O	LCD pixel data output bit 16.
	EBI_nCS0	O	External I/O chip select bank 0.
38	PA.15	I/O	General purpose digital I/O pin Port A Pin 15.
	LCD_DATA15	O	LCD pixel data output bit 15.
	PWM3	O	PWM3 output pin.
39	PA.14	I/O	General purpose digital I/O pin Port A Pin 14.
	LCD_DATA14	O	LCD pixel data output bit 14.
	PWM2	O	PWM2 output pin.
40	PA.13	I/O	General purpose digital I/O pin Port A Pin 13.
	LCD_DATA13	O	LCD pixel data output bit 13.
	PWM1	O	PWM1 output pin.
41	PA.12	I/O	General purpose digital I/O pin Port A Pin 12.
	LCD_DATA12	O	LCD pixel data output bit 12.
	PWM0	O	PWM0 output pin.
42	PA.11	I/O	General purpose digital I/O pin Port A Pin 11.
	LCD_DATA11	O	LCD pixel data output bit 11.
43	PA.10	I/O	General purpose digital I/O pin Port A Pin 10.
	LCD_DATA10	O	LCD pixel data output bit 10.
44	IO_VDD	P	MCU I/O power pin.
45	PA.9	I/O	General purpose digital I/O pin Port A Pin 9.
	LCD_DATA9	O	LCD pixel data output bit 9.
	PWRON_SET9	IU	Power On Setting bit 9.
46	PA.8	I/O	General purpose digital I/O pin Port A Pin 8.
	LCD_DATA8	O	LCD pixel data output bit 8.
	PWRON_SET8	IU	Power On Setting bit 8.
47	PA.7	I/O	General purpose digital I/O pin Port A Pin 7.
	LCD_DATA7	O	LCD pixel data output bit 7.

	PWRON_SET7	IU	Power On Setting bit 7.
48	PA.6	I/O	General purpose digital I/O pin Port A Pin 6.
	LCD_DATA6	O	LCD pixel data output bit 6.
	PWRON_SET6	IU	Power On Setting bit 6.
49	PA.5	I/O	General purpose digital I/O pin Port A Pin 5.
	LCD_DATA5	O	LCD pixel data output bit 5.
	PWRON_SET5	IU	Power On Setting bit 5.
50	PA.4	I/O	General purpose digital I/O pin Port A Pin 4.
	LCD_DATA4	O	LCD pixel data output bit 4.
	PWRON_SET4	IU	Power On Setting bit 4.
51	PA.3	I/O	General purpose digital I/O pin Port A Pin 3.
	LCD_DATA3	O	LCD pixel data output bit 3.
	PWRON_SET3	IU	Power On Setting bit 3.
52	PA.2	I/O	General purpose digital I/O pin Port A Pin 2.
	LCD_DATA2	O	LCD pixel data output bit 2.
	PWRON_SET2	IU	Power On Setting bit 2.
53	PA.1	I/O	General purpose digital I/O pin Port A Pin 1.
	LCD_DATA1	O	LCD pixel data output bit 1.
	PWRON_SET1	IU	Power On Setting bit 1.
54	PA.0	I/O	General purpose digital I/O pin Port A Pin 0.
	LCD_DATA0	O	LCD pixel data output bit 0.
	PWRON_SET0	IU	Power On Setting bit 0.
55	ADC0	I	ADC input channel 0 or VBAT.
56	ADC6	I	ADC input channel 6 or XM.
57	ADC4	I	ADC input channel 4 or YM.
58	AVSS	P	Ground pin for analog circuit.
59	AVDD	P	Power supply for internal analog circuit.
60	ADC7	I	ADC input channel 7 or XP.
61	ADC5	I	ADC input channel 5 or YP.
62	ADC1	I	ADC input channel 1.
63	ADC3	I	ADC input channel 3 or VSENSE.

64	ADC2	I	ADC input channel 2.
65	VREF	I	ADC voltage reference pin.
66	RTC_VDD	P	RTC power input. (*. or 3.3V)
67	SYS_PWREN	O	RTC wake-up output pin for external DC/DC enable pin control.
68	SYS_nWAKEUP	I	RTC wake-up interrupt input with internal pull-high.
69	X32_IN	I	External 32.768kHz crystal input.
70	X32_OUT	O	External 32.768kHz crystal output.
71	PH.4	I/O	General purpose digital I/O pin Port H Pin 4.
	UART1_TXD	O	Data transmitter output pin for UART1.
	EBI_ADDR0	O	External I/O address bus bit 0.
	INT4	I	External interrupt 4 input pin.
72	PH.5	I/O	General purpose digital I/O pin Port H Pin 5.
	UART1_RXD	I	Data receiver input pin for UART1.
	EBI_ADDR1	O	External I/O address bus bit 1.
	INT5	I	External interrupt 5 input pin.
73	PH.6	I/O	General purpose digital I/O pin Port H Pin 6.
	SD1_CMD	O	SD/SDIO Port 1 – command/response.
	UART1_RTS	O	Request to send output pin for UART1.
	EBI_ADDR2	O	External I/O address bus bit 2.
	INT6	I	External interrupt 6 input pin.
74	PH.7	I/O	General purpose digital I/O pin Port H Pin 7.
	SD1_CLK	O	SD/SDIO Port 1 – clock.
	UART1_CTS	I	Clear to send input pin for UART1.
	EBI_ADDR3	O	External I/O address bus bit 3.
	INT7	I	External interrupt 7 input pin.
75	PH.8	I/O	General purpose digital I/O pin Port H Pin 8.
	SD1_DAT0	I/O	SD/SDIO mode #1 data line bit 0.
	UART4_TXD	O	Data transmitter output pin for UART4.
	EBI_ADDR4	O	External I/O address bus bit 4.
76	PH.9	I/O	General purpose digital I/O pin Port H Pin 9.
	SD1_DAT1	I/O	SD/SDIO mode #1 data line bit 1.

	UART4_RXD	I	Data receiver input pin for UART4.
	EBI_ADDR5	O	External I/O address bus bit 5.
77	PH.10	I/O	General purpose digital I/O pin Port H Pin 10.
	SD1_DAT2	I/O	SD/SDIO mode #1 data line bit 2.
	UART4_RTS	O	Request to send output pin for UART4.
	EBI_ADDR6	O	External I/O address bus bit 6.
78	PH.11	I/O	General purpose digital I/O pin Port H Pin 11.
	SD1_DAT3	I/O	SD/SDIO mode #1 data line bit 3.
	UART4_CTS	I	Clear to send input pin for UART4.
	EBI_ADDR7	O	External I/O address bus bit 7.
79	PH.12	I/O	General purpose digital I/O pin Port H Pin 12.
	SD1_nCD	I	SD/SDIO mode #1 – card detect.
	UART8_TXD	O	Data transmitter output pin for UART8.
	SPI0_SS1	O	2nd SPI0 chip select pin.
	EBI_ADDR8	O	External I/O address bus bit 8.
80	IO_VDD	P	MCU I/O power pin.
81	CORE_VSS	P	MCU internal core ground pin.
82	CORE_VDD	P	MCU internal core power pin.
83	PH.13	I/O	General purpose digital I/O pin Port H Pin 13.
	SD1_nPWR	O	SD/SDIO mode #1 – power enable.
	UART8_RXD	I	Data receiver input pin for UART8.
	SPI1_SS1	O	2nd SPI1 chip select pin.
	EBI_ADDR9	O	External I/O address bus bit 9.
84	PH.14	I/O	General purpose digital I/O pin Port H Pin 14.
	UART8_RTS	O	Request to send output pin for UART8.
	EBI_nBE0	O	External I/O low byte enable.
85	PH.15	I/O	General purpose digital I/O pin Port H Pin 15.
	UART8_CTS	I	Clear to send input pin for UART8.
	EBI_nBE1	O	External I/O high byte enable.
86	PI.0	I/O	General purpose digital I/O pin Port I Pin 0.
	EBI_DATA0	I/O	External I/O data bus bit 0.

87	PI.1	I/O	General purpose digital I/O pin Port I Pin 1.
	NAND_nCS0	O	NAND flash chip select 0.
	UART7_TXD	O	Data transmitter output pin for UART7.
	EBI_DATA1	I/O	External I/O data bus bit 1.
	INT6	I	External interrupt 6 input pin.
88	PI.2	I/O	General purpose digital I/O pin Port I Pin 2.
	NAND_nWP	O	NAND flash srite protect.
	UART7_RXD	I	Data receiver input pin for UART7.
	EBI_DATA2	I/O	External I/O data bus bit 2.
	INT7	I	External interrupt 7 input pin.
89	PI.3	I/O	General purpose digital I/O pin Port I Pin 3.
	NAND_ALE	O	NAND flash address latch enable.
	I2C1_SCL	O	I^2C1 clock pin.
	EBI_DATA3	I/O	External I/O data bus bit 3.
	RTC_TICK	O	RTC tick output
90	PI.4	I/O	General purpose digital I/O pin Port I Pin 4.
	NAND_CLE	O	NAND flash command latch enable.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
	EBI_DATA4	I/O	External I/O data bus bit 4.
91	PI.5	I/O	General purpose digital I/O pin Port I Pin 5.
	NAND_nWE	O	NAND flash write enable.
	eMMC_CMD	I/O	eMMC command/Response.
	EBI_DATA5	I/O	External I/O data bus bit 5.
	SD1_CMD	O	SD/SDIO mode #1 – command/response.
	UART1_TXD	O	Data transmitter output pin for UART1.
	SPI1_SS0	O	1st SPI1 chip select pin.
92	PI.6	I/O	General purpose digital I/O pin Port I Pin 6.
	NAND_nRE	O	NAND flash read enable.
	eMMC_CLK	O	eMMC clock output.
	SC1_RST	O	SmartCard1 reset pin.
	EBI_DATA6	I/O	External I/O data bus bit 6.

	SD1_CLK	O	SD/SDIO mode #1– clock.
	UART1_RXD	I	Data receiver input pin for UART1.
	SPI1_CLK	O	SPI1 serial clock pin.
93	PI.7	I/O	General purpose digital I/O pin Port I Pin 7.
	NAND_RDY0	I	NAND flash ready/busy channel 0.
	eMMC_DATA3	I/O	eMMC data line bit 3.
	SC1_CLK	O	SmartCard1 clock pin.
	EBI_DATA7	I/O	External I/O data bus bit 7.
	SD1_DAT0	I/O	SD/SDIO mode #1 data line bit 0.
	UART1_RTS	O	Request to send output pin for UART1.
	SPI1_DO (SPI1_DATA0)	I (I/O)	SPI1 Data out pin. (SPI1 data 0 in dual/quad mode.)
94	PI.8	I/O	General purpose digital I/O pin Port I Pin 8.
	NAND_DATA0	I/O	NAND flash data bus bit 0.
	eMMC_DATA0	I/O	eMMC data line bit 0.
	SC1_DAT	I/O	SmartCard1 data pin.
	EBI_DATA8	I/O	External I/O data bus bit 8.
	SD1_DAT1	I/O	SD/SDIO mode #1 data line bit 1.
	UART1_CTS	I	Clear to send input pin for UART1.
	SPI1_DI (SPI1_DATA1)	I (I/O)	SPI1 Data input pin. (SPI1 data 1 in dual/quad mode.)
95	PI.9	I/O	General purpose digital I/O pin Port I Pin 9.
	NAND_DATA1	I/O	NAND flash data bus bit 1.
	eMMC_DATA1	I/O	eMMC data line bit 1.
	SC1_PWR	O	SmartCard1 power pin.
	EBI_DATA9	I/O	External I/O data bus bit 9.
	SD1_DAT2	I/O	SD/SDIO mode #1 data line bit 2.
	UART4_TXD	O	Data transmitter output pin for UART4.
96	PI.10	I/O	General purpose digital I/O pin Port I Pin 10.
	NAND_DATA2	I/O	NAND flash data bus bit 2.
	eMMC_DATA2	I/O	eMMC data line bit 2.

	SC1_CD	I	SmartCard1 card detect pin.
	EBI_DATA10	I/O	External I/O data bus bit 10.
	SD1_DAT3	I/O	SD/SDIO mode #1 data line bit 3.
	UART4_RXD	I	Data receiver input pin for UART4.
97	PI.11	I/O	General purpose digital I/O pin Port I Pin 11.
	NAND_DATA3	I/O	NAND flash data bus bit 3.
	SC0_RST	O	SmartCard0 reset pin.
	EBI_DATA11	I/O	External I/O data bus bit 11.
98	PI.12	I/O	General purpose digital I/O pin Port I Pin 12.
	NAND_DATA4	I/O	NAND flash data bus bit 4.
	UART8_TXD	O	Data transmitter output pin for UART8.
	SC0_CLK	O	SmartCard0 clock pin.
	EBI_DATA12	I/O	External I/O data bus bit 12.
	SD1_nCD	I	SD/SDIO mode #1 – card detect.
99	PI.13	I/O	General purpose digital I/O pin Port I Pin 13.
	NAND_DATA5	I/O	NAND flash data bus bit 5.
	UART8_RXD	I	Data receiver input pin for UART8.
	SC0_DAT	I/O	SmartCard0 data pin.
	EBI_DATA13	I/O	External I/O data bus bit 13.
	SD1_nPWR	O	SD/SDIO mode #1 – power enable.
100	PI.14	I/O	General purpose digital I/O pin Port I Pin 14.
	NAND_DATA6	I/O	NAND flash data bus bit 6.
	UART8_RTS	O	Request to send output pin for UART8.
	SC0_PWR	O	SmartCard0 power pin.
	EBI_DATA14	I/O	External I/O data bus bit 14.
101	PI.15	I/O	General purpose digital I/O pin Port I Pin 15.
	NAND_DATA7	I/O	NAND flash data bus bit 7.
	UART8_CTS	I	Clear to send input pin for UART8.
	SC0_CD	I	SmartCard0 card detect pin.
	EBI_DATA15	I/O	External I/O data bus bit 15.
	CLK_OUT	O	Clock output pin.

102	CORE_VDD	P	MCU internal core power pin.
103	CORE_VSS	P	MCU internal core ground pin.
104	IO_VDD	P	MCU I/O power pin.
105	PB.0	I/O	General purpose digital I/O pin Port B Pin 0.
	NAND_nCS1	O	NAND flash chip select 1.
	UART5_TXD	O	Data transmitter output pin for UART5.
	SPI0_SS1	O	2nd SPI0 chip select pin.
	TM1_TGL	O	Enhanced TIMER toggle output pin.
106	PB.1	I/O	General purpose digital I/O pin Port B Pin 1.
	NAND_RDY1	I	NAND flash ready/busy channel 1.
	UART5_RXD	I	Data receiver input pin for UART5.
	SPI1_SS1	O	2nd SPI1 chip select pin.
	TM1_CAP	I	Enhanced TIMER capture input pin.
107	PB.2	I/O	General purpose digital I/O pin Port B Pin 2.
	UART6_TXD	O	Data transmitter output pin for UART6.
	PWM0	O	PWM0 output pin.
	TM0_TGL	O	Enhanced TIMER toggle output pin.
108	PB.3	I/O	General purpose digital I/O pin Port B Pin 3.
	UART6_RXD	I	Data receiver input pin for UART6.
	PWM1	O	PWM1 output pin.
	TM0_CAP	I	Enhanced TIMER capture input pin.
109	PB.4	I/O	General purpose digital I/O pin Port B Pin 4.
	UART6_RTS	O	Request to send output pin for UART6.
110	PB.5	I/O	General purpose digital I/O pin Port B Pin 5.
	UART6_CTS	I	Clear to send input pin for UART6.
111	PB.6	I/O	General purpose digital I/O pin Port B Pin 6.
	SPI0_SS0	O	1st SPI0 chip select pin.
112	PB.7	I/O	General purpose digital I/O pin Port B Pin 7.
	SPI0_CLK	O	SPI0 serial clock pin.
113	PB.8	I/O	General purpose digital I/O pin Port B Pin 8.
	SPI0_DO (SPI0_DATA0)	O (I/O)	SPI0 Data out pin. (SPI0 data 0 in dual/quad mode.)

114	PB.9	I/O	General purpose digital I/O pin Port B Pin 9.
	SPI0_DI (SPI0_DATA1)	I (I/O)	SPI0 Data input pin. (SPI0 data 1 in dual/quad mode.)
115	PB.10	I/O	General purpose digital I/O pin Port B Pin 10.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI0_DATA2	I/O	SPI0 data 2 in dual/quad mode.
	CAN0_RXD	I	CAN bus receiver0 input.
116	PB.11	I/O	General purpose digital I/O pin Port B Pin 11.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI0_DATA3	I/O	SPI0 data 3 in dual/quad mode.
	CAN0_TXD	O	CAN bus transmitter0 output.
117	PB.12	I/O	General purpose digital I/O pin Port B Pin 12.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI1_SS0	O	1st SPI1 chip select pin.
118	PB.13	I/O	General purpose digital I/O pin Port B Pin 13.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI1_CLK	O	SPI1 serial clock pin.
119	PB.14	I/O	General purpose digital I/O pin Port B Pin 14.
	UART10_RTS	O	Request to send output pin for UART10.
	SPI1_DO (SPI1_DATA0)	O (I/O)	SPI1 Data out pin. (SPI1 data 0 in dual/quad mode.)
120	PB.15	I/O	General purpose digital I/O pin Port B Pin 15.
	UART10_CTS	I	Clear to send input pin for UART10.
	SPI1_DI (SPI1_DATA1)	I (I/O)	SPI1 Data input pin. (SPI1 data 1 in dual/quad mode.)
121	PG.4	I/O	General purpose digital I/O pin Port G Pin 4.
	NAND_nCS1	O	NAND flash chip select 1.
	UART7_TXD	O	Data transmitter output pin for UART7.
	SPI1_DATA2	I/O	SPI1 data 2 in dual/quad mode.
122	PG.5	I/O	General purpose digital I/O pin Port G Pin 5.

	NAND_RDY1	I	NAND flash ready/busy channel 1.
	UART7_RXD	I	Data receiver input pin for UART7.
	SPI1_DATA3	I/O	SPI1 data 3 in dual/quad mode.
123	PC.0	I/O	General purpose digital I/O pin Port C Pin 0.
	NAND_DATA0	I/O	NAND flash data bus bit 0.
	eMMC_DATA0	I/O	eMMC data line bit 0.
124	PC.1	I/O	General purpose digital I/O pin Port C Pin 1.
	NAND_DATA1	I/O	NAND flash data bus bit 1.
	eMMC_DATA1	I/O	eMMC data line bit 1.
125	PC.2	I/O	General purpose digital I/O pin Port C Pin 2.
	NAND_DATA2	I/O	NAND flash data bus bit 2.
	eMMC_DATA2	I/O	eMMC data line bit 2.
126	PC.3	I/O	General purpose digital I/O pin Port C Pin 3.
	NAND_DATA3	I/O	NAND flash data bus bit 3.
	eMMC_DATA3	I/O	eMMC data line bit 3.
127	PC.4	I/O	General purpose digital I/O pin Port C Pin 4.
	NAND_DATA4	I/O	NAND flash data bus bit 4.
	eMMC_CMD	I/O	eMMC command/Response.
128	PC.5	I/O	General purpose digital I/O pin Port C Pin 5.
	NAND_DATA5	I/O	NAND flash data bus bit 5.
	eMMC_CLK	O	eMMC clock output.
129	PC.6	I/O	General purpose digital I/O pin Port C Pin 6.
	NAND_DATA6	I/O	NAND flash data bus bit 6.
	UART10_TXD	O	Data transmitter output pin for UART10.
	TM0_TGL	O	Enhanced TIMER toggle output pin.
130	PC.7	I/O	General purpose digital I/O pin Port C Pin 7.
	NAND_DATA7	I/O	NAND flash data bus bit 7.
	UART10_RXD	I	Data receiver input pin for UART10.
	TM0_CAP	I	Enhanced TIMER capture input pin.
131	PC.8	I/O	General purpose digital I/O pin Port C Pin 8.
	NAND_nCS0	O	NAND flash chip select 0.

	UART10_RTS	O	Request to send output pin for UART10.
	TM1_TGL	O	Enhanced TIMER toggle output pin.
132	PC.9	I/O	General purpose digital I/O pin Port C Pin 9.
	NAND_ALE	O	NAND flash address latch enable.
	UART10_CTS	I	Clear to send input pin for UART10.
	TM1_CAP	I	Enhanced TIMER capture input pin.
133	PC.10	I/O	General purpose digital I/O pin Port C Pin 10.
	NAND_CLE	O	NAND flash command latch enable.
	UART4_TXD	O	Data transmitter output pin for UART4.
	TM2_TGL	O	Enhanced TIMER toggle output pin.
134	PC.11	I/O	General purpose digital I/O pin Port C Pin 11.
	NAND_nWE	O	NAND flash write enable.
	UART4_RXD	I	Data receiver input pin for UART4.
	TM2_CAP	I	Enhanced TIMER capture input pin.
135	PC.12	I/O	General purpose digital I/O pin Port C Pin 12.
	NAND_nRE	O	NAND flash read enable.
	UART4_RTS	O	Request to send output pin for UART4.
	TM3_TGL	O	Enhanced TIMER toggle output pin.
136	PC.13	I/O	General purpose digital I/O pin Port C Pin 13.
	NAND_RDY0	I	NAND flash ready/busy channel 0.
	UART4_CTS	I	Clear to send input pin for UART4.
	TM3_CAP	I	Enhanced TIMER capture input pin.
137	PC.14	I/O	General purpose digital I/O pin Port C Pin 14.
	NAND_nWP	O	NAND flash write protect.
	PWM0	O	PWM0 output pin.
138	PJ.3	I/O	General purpose digital I/O pin Port J Pin 3.
	JTAG_TDO	O	JTAG test data out.
139	PJ.0	I/O	General purpose digital I/O pin Port J Pin 0.
	JTAG_TCK	O	JTAG test clock.
140	PJ.1	I/O	General purpose digital I/O pin Port J Pin 1.
	JTAG_TMS	O	JTAG test mode select.

141	PJ.2	I/O	General purpose digital I/O pin Port J Pin 2.
	JTAG_TDI	I	JTAG test data in.
142	PJ.4	I/O	General purpose digital I/O pin Port J Pin 4.
	JTAG_nTRST	O	JTAG Reset.
143	nRESET	IU	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
	WDT_nRST	O	Watch dog timer external reset output pin. Open-drain.
144	IO_VDD	P	MCU I/O power pin.
145	CORE_VSS	P	MCU internal core ground pin.
146	CORE_VDD	P	MCU internal core power pin.
147	DDR_VSS	P	DDR ground pin.
148	DDR_VDD	P	DDR power pin.
149	DDR_VSS	P	DDR ground pin.
150	DDR_VDD	P	DDR power pin.
151	DDR_VSS	P	DDR ground pin.
152	DDR_VDD	P	DDR power pin.
153	CORE_VSS	P	MCU internal core ground pin.
154	IO_VDD	P	MCU I/O power pin.
155	PD.0	I/O	General purpose digital I/O pin Port D Pin 0.
	SD0_CMD	O	SD/SDIO mode #0 command/response.
156	PD.1	I/O	General purpose digital I/O pin Port D Pin 1.
	SD0_CLK	O	SD/SDIO mode #0 clock.
157	PD.2	I/O	General purpose digital I/O pin Port D Pin 2.
	SD0_DAT0	I/O	SD/SDIO mode #0 data line bit 0.
158	PD.3	I/O	General purpose digital I/O pin Port D Pin 3.
	SD0_DAT1	I/O	SD/SDIO mode #0 data line bit 1.
159	PD.4	I/O	General purpose digital I/O pin Port D Pin 4.
	SD0_DAT2	I/O	SD/SDIO mode #0 data line bit 2.
160	PD.5	I/O	General purpose digital I/O pin Port D Pin 5.
	SD0_DAT3	I/O	SD/SDIO mode #0 data line bit 3.
161	PD.6	I/O	General purpose digital I/O pin Port D Pin 6.
	SD0_nCD	I	SD/SDIO mode #0 card detect.

162	PD.7	I/O	General purpose digital I/O pin Port D Pin 7.
163	CORE_VDD	P	MCU internal core power pin.
164	PLL_VDD	P	PLL power input pin.
165	PLL_VSS	P	PLL ground.
166	CORE_VDD	P	MCU internal core power pin.
167	PH.3	I/O	General purpose digital I/O pin Port H Pin 3.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM3	O	PWM3 output pin.
	INT3	I	External interrupt 3 input pin.
168	PH.2	I/O	General purpose digital I/O pin Port H Pin 2.
	I2C1_SCL	O	I^2C1 clock pin.
	UART9_TXD	O	Data transmitter output pin for UART9.
	PWM2	O	PWM2 output pin.
	INT2	I	External interrupt 2 input pin.
169	PE.13	I/O	General purpose digital I/O pin Port E Pin 13.
	UART8_CTS	I	Clear to send input pin for UART8.
	UART3_RXD	I	Data receiver input pin for UART3.
	CLK_OUT	O	Reference Clock Output.
170	PE.12	I/O	General purpose digital I/O pin Port E Pin 12.
	UART8_RTS	O	Request to send output pin for UART8.
	UART3_TXD	O	Data transmitter output pin for UART3.
171	PE.11	I/O	General purpose digital I/O pin Port E Pin 11.
	UART8_RXD	I	Data receiver input pin for UART8.
172	PE.10	I/O	General purpose digital I/O pin Port E Pin 10.
	UART8_TXD	O	Data transmitter output pin for UART8.
173	PE.9	I/O	General purpose digital I/O pin Port E Pin 9.
	SD1_nPWR	O	SD/SDIO mode #1 power enable.
	UART1_CD	I	Carrier detect input pin for UART1.
174	PE.8	I/O	General purpose digital I/O pin Port E Pin 8.
	SD1_nCD	I	SD/SDIO mode #1 card detect.

	UART1_RI	I	Ring indicator input pin for UART1.
175	PE.7	I/O	General purpose digital I/O pin Port E Pin 7.
	SD1_DAT3	I/O	SD/SDIO mode #1 data line bit 3.
	UART1_DSR	I	Data set ready input pin for UART1.
176	PE.6	I/O	General purpose digital I/O pin Port E Pin 6.
	SD1_DAT2	I/O	SD/SDIO mode #1 data line bit 2.
	UART1_DTR	O	Data terminal ready output pin for UART1.
177	PE.5	I/O	General purpose digital I/O pin Port E Pin 5.
	SD1_DAT1	I/O	SD/SDIO mode #1 data line bit 1.
	UART1_CTS	I	Clear to send input pin for UART1.
	CLK_OUT	O	Reference Clock Output.
178	PE.4	I/O	General purpose digital I/O pin Port E Pin 4.
	SD1_DAT0	I/O	SD/SDIO mode #1 ata line bit 0.
	UART1_RTS	O	Request to send output pin for UART1.
179	PE.3	I/O	General purpose digital I/O pin Port E Pin 3.
	SD1_CLK	O	SD/SDIO mode #1 clock.
	UART1_RXD	I	Data receiver input pin for UART1.
180	PE.2	I/O	General purpose digital I/O pin Port E Pin 2.
	SD1_CMD	O	SD/SDIO mode #1 command/response.
	UART1_TXD	O	Data transmitter output pin for UART1.
181	PE.1	I/O	General purpose digital I/O pin Port E Pin 1.
	UART0_RXD	I	Data receiver input pin for UART0.
182	PE.0	I/O	General purpose digital I/O pin Port E Pin 0.
	UART0_TXD	O	Data transmitter output pin for UART0.
183	IO_VDD	P	MCU I/O power pin.
184	XT1_IN	I	External 12MHz crystal input pin.
185	XT1_OUT	O	External 12MHz crystal output pin.
186	IO_VSS	P	MCU I/O ground pin.
187	PF.9	I/O	General purpose digital I/O pin Port F Pin 9.
188	PF.8	I/O	General purpose digital I/O pin Port F Pin 8.
189	PF.7	I/O	General purpose digital I/O pin Port F Pin 7.

190	PF.6	I/O	General purpose digital I/O pin Port F Pin 6.
191	PF.5	I/O	General purpose digital I/O pin Port F Pin 5.
192	PF.4	I/O	General purpose digital I/O pin Port F Pin 4.
193	PF.3	I/O	General purpose digital I/O pin Port F Pin 3.
194	PF.2	I/O	General purpose digital I/O pin Port F Pin 2.
195	PF.1	I/O	General purpose digital I/O pin Port F Pin 1.
196	PF.0	I/O	General purpose digital I/O pin Port F Pin 0.
197	PH.1	I/O	General purpose digital I/O pin Port H Pin 1.
	USB_OVRCUR	I	USB overcurrent
	INT1	I	External interrupt 1 input pin.
198	PH.0	I/O	General purpose digital I/O pin Port H Pin 0.
	USB0_VBUSVLD	I	USB0 VBUS valid.
	INT0	I	External interrupt 0 input pin.
199	PF.10	I/O	General purpose digital I/O pin Port F Pin 10.
	USB_PWREN	O	USB host output power control pin for LQFP128 package only.
200	PE.15	I/O	General purpose digital I/O pin Port E Pin 15.
	USB1_PWREN	O	USB1 host output power control pin.
201	PE.14	I/O	General purpose digital I/O pin Port E Pin 14.
	USB0_PWREN	O	USB0 host output power control pin.
202	CORE_VSS	P	MCU internal core ground pin.
203	CORE_VDD	P	MCU internal core power pin.
204	USBPLL1_VDD	P	USB1 PLL power pin.
205	USB1_VSS	P	USB1 ground pin.
206	USB1_DM	I/O	USB1 differential signal D-.
207	USB1_DP	I/O	USB1 differential signal D+.
208	USB1_VDD	P	USB1 I/O power pin.
209	USB1_REXT	I	USB1 module reference Resister.
210	USBPLL0_VDD	P	USB0 PLL power pin.
211	USB0_VSS	P	USB0 ground pin.
212	USB0_DM	I/O	USB0 differential signal D-.
213	USB0_DP	I/O	USB0 differential signal D+.

214	USB0_VDD	P	USB0 I/O power pin.
215	USB0_REXT	I	USB0 module reference Resister.
216	USB0_ID	IU	USB0 Host/Device select.

Note: Pin Type I=Digital Input; IU=Digital Input with internal pull high, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

5 BLOCK DIAGRAM

5.1 N9H30 Series Block Diagram

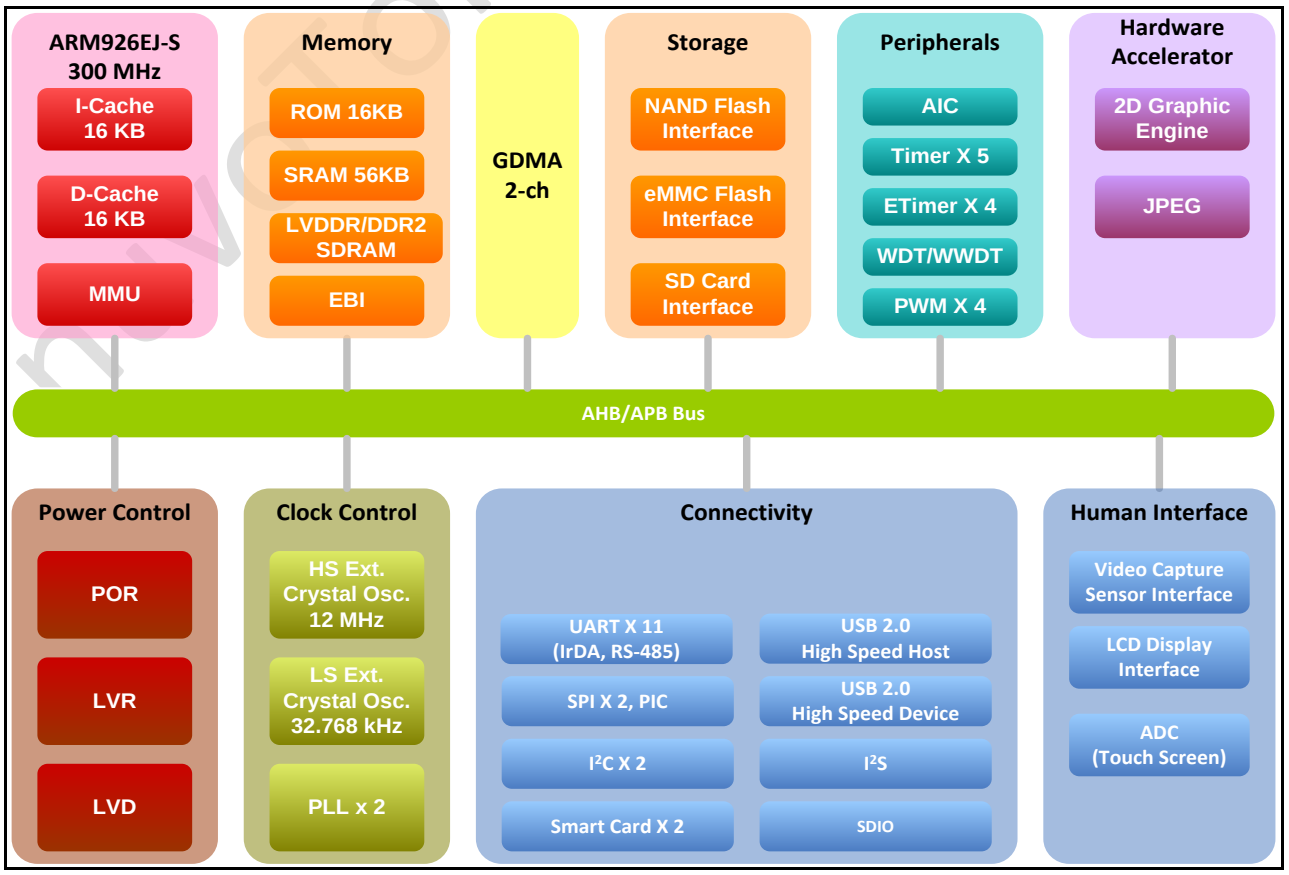


Figure 4.1 N9H30 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® ARM926EJ-S CPU Core

6.1.1 Overview

The ARM926EJ-S CPU core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S CPU core is targeted at multi-tasking applications where full memory management, high performance, and low power are all important.

The ARM926EJ-S CPU core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to choose between high performance and high code density. The ARM926EJ-S CPU core includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead.

The ARM926EJ-S processor provides support for external coprocessor enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S CPU core implements ARM architecture version 5TEJ.

The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core.
- A Memory Management Unit (MMU).
- Separate instruction and data cache.
- Separate instruction and data AMBA AHB bus interfaces.

6.2 System Manager

6.2.1 Overview

The system management describes following information and functions.

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Product Identifier (PDID), Power-On Setting, System Wake-Up, Reset Control for on-chip controllers/peripherals, and multi-function pin control.
- System Control registers

6.3 Clock Controller (CLK_CTL)

6.3.1 Overview

The clock controller generates all clocks for Video, Audio, CPU, AMBA and all the engine modules. This chip includes two PLL modules. The clock source for each module comes from the PLL, or from the external crystal input directly. For each clock there is bit on the CLKEN register to control the clock ON or OFF individually, and the divider setting is on the CLK_DIVCTL register. The register can also be used to control the clock enable or disable for power control.

6.4 Advanced Interrupt Controller (AIC)

6.4.1 Overview

An interrupt temporarily changes the sequence of program execution to react to a particular event such as power failure, watchdog timer timeout and so on. The CPU processor provides two modes of interrupt, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general purpose. The IRQ request is occurred when the nIRQ input is asserted. Similarly, the FIQ request is occurred when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F and I bits in the current program status register (CPSR).

6.5 SDRAM Interface Controller (SDIC)

6.5.1 Overview

The SDRAM Controller support DDR and DDR2 type SDRAM. Only 16-bit data bus width is supported.

The SDRAM controller interface to three isolated AHB. All these AHB masters can access the memory independent. Except the memory access, the masters of AHB also could access the SDRAM control registers.

6.6 MTP Controller (MTP)

6.6.1 Overview

The MTP (Multi-Time Programmable) controller performs an easy way to use and program the 256-bit Key for IP Security Engine. There is a MTP EPROM in this chip, and it can be programmed 15 times. User can program 256-bit key and 8-bit user defined fields each time. The 256-bit key is program-only, and only can be used by IP Security Engine. User can use the 8-bit user defined field for special purpose. The MTP also supports a LOCK function to protect the content of programmed key and user defined field.

6.7 General Purpose I/O (GPIO)

6.7.1 Overview

The N9H30 series have up to 86 General-Purpose I/O (GPIO) pins and can be shared with other function pins depending on the chip configuration.

6.8 General DMA Controller (GDMA)

6.8.1 Overview

The chip has a two-channel general DMA controller with or without descriptor fetch operation, called the GDMA. The two-channel GDMA performs the memory-to-memory data transfers without the CPU intervention:

6.9 Timer Controller (TMR)

6.9.1 Overview

The general timer controller includes five channels, TIMER0, TIMER1, TIMER2, TIMER3, and TIMER4, which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, pulse generation, delay timing, and so on. The timer possesses features such as adjustable resolution, programmable counting period, and detailed information. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

6.10 Enhance Timer Controller (ETMR)

6.10.1 Overview

This chip is equipped with four enhance timer modules including ETIMER0, ETIMER1, ETIMER2 and ETIMER3, which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

6.11 Pulse Width Modulation (PWM)

6.11.1 Overview

This chip has one PWM controller, and it has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators. Each PWM pair has one Prescaler, one clock divider, two clock selectors, two 16-bit PWM counters, two 16-bit comparators, and one Dead-Zone generator. They are all driven by APB system clock (PCLK) in chip. Each PWM channel can be used as a timer and issue interrupt independently.

6.12 Watchdog Timer (WDT)

6.12.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.13 Windowed Watchdog Timer (WWDT)

6.13.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.14 Real Time Clock (RTC)

6.14.1 Overview

The Real Time Clock (RTC) controller provides the real time clock and calendar information. The clock source of RTC controller is from an external 32.768 kHz low-speed crystal which connected at pins X32_IN and X32_OUT (refer to pin Description). The RTC controller provides the real time clock (hour, minute, second) in RTC_TIME (RTC Time Loading Register) as well as calendar information (year, month, day) in RTC_CAL (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in RTC_TALM (RTC Time Alarm Register) and alarm calendar in RTC_CALM (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD (Binary Coded Decimal) format.

6.15 UART Interface Controller (UART)

6.15.1 Overview

This chip equips up to 9 channels of Universal Asynchronous Receiver/Transmitters (UART). UART1/4/6/8/10 supports High-speed UART and UART0/5/7/9 perform Normal Speed UART, besides, all the UART channels support flow control function. The UART controller also supports IrDA (SIR), LIN Master/Slave and RS-485 function modes.

6.16 Smart Card Host Interface (SC)

6.16.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.17 I^2C Synchronous Serial Interface Controller (I^2C)

6.17.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.18 SPI Interface Controller (SPI)

6.18.1 Overview

The SPI is a synchronous serial interface performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from CPU. This interface can drive up to 2 external peripherals and is seen as the master.

6.19 I^2S Controller (I^2S)

6.19.1 Overview

The I^2S controller consists of I^2S and PCM protocols to interface with external audio CODEC. The I^2S and PCM interface supports 8, 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

6.20 USB 2.0 Device Controller (USBD)

6.20.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.21 USB Host Controller (USBH)

6.21.1 Overview

The Universal Serial Bus (USB) is a fast, bi-directional, isochronous, low-cost, dynamically attachable serial interface standard intended for modem, scanners, PDAs, keyboards, mice, and digital imaging devices. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and a network of peripheral devices. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

6.22 Flash Memory Interface (FMI)

6.22.1 Overview

The Flash Memory Interface (FMI) of this Chip has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (ex. SDRAM) and shared buffer (128 bytes), and the FMI unit control the interface of eMMC or NAND flash. The interface controller can support eMMC and NAND-type flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.23 Secure Digital Host Controller (SDH)

6.23.1 Overview

The Secure-Digital Card Host Controller (SDH) equips DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC/SDIO. The SDH controller supports SD/SDHC/SDIO card and cooperates with DMAC to provide a fast data transfer between system memory and cards.

6.24 2D Graphic Engine (GE2D)

6.24.1 Overview

A 32-bit 2D Graphics Engine (GE2D) is specially designed to improve the performance of graphic processing. It can accelerate the operation of individual GUI functions such as BitBLTs and Bresenham Line Draw to operate at all pixel depths including 8/16/32 bit-per-pixel.

6.25 JPEG Codec (JPEG)

6.25.1 Overview

The JPEG Codec supports Baseline Sequential Mode JPEG still image compression and decompression that is fully compliant with ISO/IEC International Standard 10918-1 (T.81). The features and capability of the JPEG codec are listed below.

6.26 LCD Display Interface Controller (LCM)

6.26.1 Overview

The main purpose of Display Controller is used to display the video/image data to LCD device or connect with external TV-encoder. The data source may come from the JPEG decoder and the OSD pattern which have been stored in system memory (SDRAM). The input data format of the display controller can be packet YUV422, packet YUV444, packet RGB444, packet RGB565, packet RGB666, and packet RGB888. The OSD (On Screen Display) function supports packet YUV422 and 8/16-bit direct-color mode. The LCD controller supports both sync-type and MPU-type LCDM. This LCD Controller is a bus master and can transfer display data from system memory (SDRAM) without CPU intervention.

6.27 Analog to Digital Converter (ADC)

6.27.1 Overview

The N9H30 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with 5 input channels. The A/D converter supports two operation modes: 4-wire or 5-wire mode. The ADC is especially suitable to act as touch screen controller.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
V_{CORE_VDD}–V_{CORE_VSS}	Core DC Power Supply	-0.3	+1.26	V
V_{IO_VDD}–V_{IO_VSS}	I/O DC Power Supply	-0.3	+3.63	V
V_{DDR_VDD}–V_{DDR_VSS}	DDR I/O DC Power Supply	-0.3	+1.90	V
V_{IN}	Input Voltage	V_{IO_VSS}-0.3	+3.6	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into CORE_VDD	-	200	mA
I_{SS}	Maximum Current out of CORE_VSS	-	200	mA
I_{IO}	Maximum Current sunk by a I/O pin	-	20	mA
	Maximum Current sourced by a I/O pin	-	30	mA
	Maximum Current sunk by total I/O pins	-	200	mA
	Maximum Current sourced by total I/O pins	-	200	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 N9H30 Series DC Electrical Characteristics

(VDD-VSS=3.3 V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Core Operation voltage	V_{CORE_VDD}	1.14	1.2	1.26	V	
I/O Operation Voltage	V_{IO_VDD}	2.97	3.3	3.63	V	
DDR I/O Operation Voltage	V_{DDR_VDD}	1.70	1.8	1.90	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	2.97	3.3	3.63	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Current Consumption of Normal Operating Mode 1	I_{CORE_VDD1}		185		mA	Frequency of CPUCLK/DDR_CLK is 300/150 MHz. The functionalities enabled are GE2D, LCD, JPEG, graphic Engine, USBD, USBH and UART.
	I_{DDR_VDD1}		40		mA	
	I_{USBPLL_VDD1}		15		mA	
	I_{USB0_VDD1}		35		mA	
	I_{USB1_VDD1}		35		mA	
	I_{RTC_VDD1}		100		uA	
Current Consumption of Normal Operating Mode 2	I_{CORE_VDD2}		165		mA	Frequency of CPUCLK/DDR_CLK is 264/132 MHz. The functionalities enabled are GE2D, LCD, JPEG, graphic Engine, USBD, USBH and UART.
	I_{DDR_VDD2}		35		mA	
	I_{USBPLL_VDD2}		15		mA	
	I_{USB0_VDD2}		35		mA	
	I_{USB1_VDD2}		35		mA	
	I_{RTC_VDD2}		100		uA	
Current Consumption of Deep Standby Mode	$I_{STDBY\_CORE\_VDD}$		3		mA	V_{CORE_VDD} = 1.2V
	$I_{STDBY\_DDR\_VDD}$		6		mA	V_{DDR_VDD} = 1.8V
	$I_{STDBY\_IO\_VDD}$		5		µA	V_{IO_VDD} = 3.3V
	$I_{STDBY\_USB0\_VDD}$		0		µA	V_{USB0_VDD} = 3.3V
	$I_{STDBY\_USB1\_VDD}$		0		µA	V_{USB1_VDD} = 3.3V
	$I_{STDBY\_UPLL0\_VDD}$		5		µA	$V_{USBPLL0\_VDD}$ = 1.2V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	$I_{STDBY\_UPLL1\_VDD}$		5		μA	$V_{USBPLL1\_VDD}$ = 1.2V
	I_{STDBY_AVDD}		25		μA	V_{AVDD} = 3.3V
	$I_{STDBY\_RTC\_VDD}$		100		μA	V_{RTC_VDD} = 3.3V
Current Consumption of Power Down Mode	$I_{PWD\_RTC\_VDD}$		7		uA	V_{RTC_VDD} = 3.0V
Input Leakage Current PA, PB, PD, PE, PF, PC, PH, PI, PJ	I_{LK1}	-10	-	10	μA	V_{IO_VDD} = 3.63V 0V < V_{IN} < 3.6V
Input Leakage Current with Pull-Down Resistor on PA, PB, PD, PE, PF, PC, PH, PI, PJ	I_{LK2}	40	-	160	μA	V_{IN} = V_{IO_VDD}
Input Leakage Current with Pull-Up Resistor on PA, PB, PD, PE, PF, PC, PH, PI, PJ	I_{LK3}	-160	-	40	μA	V_{IN} = 0
Input Low Voltage PA, PB, PD, PE, PF, PC, PH, PI, PJ (TTL input)	V_{IL1}	-	-	0.8	V	
Input High Voltage PA, PB, PD, PE, PF, PC, PH, PI, PJ (TTL input)	V_{IH1}	2.0	-	-	V	
Input Low Voltage PA, PB, PD, PE, PF, PC, PH, PI, PJ (Schmitt input)	V_{IL2}	0.9	1.05	1.2	V	
Input High Voltage PA, PB, PD, PE, PF, PC, PH, PI, PJ (Schmitt input)	V_{IH2}	1.65	1.9	2.1	V	
Hysteresis voltage PA, PB, PD, PE, PF, PC, PH, PI, PJ (Schmitt input)	V_{HY}	0.75	0.85	0.9	V	
Negative going threshold (Schmitt input), nRESET	V_{ILS}	0.75	-	0.9	V	
Positive going threshold (Schmitt input), nRESET	V_{IHS}	1.65	-	2.1	V	
Source Current PA, PB, PD, PE, PF, PH, PI, PJ (Push-pull Mode)	I_{SR21}	8	-	28	mA	
Sink Current PA, PB, PD, PE (Push-pull Mode)	I_{SK1}	8	-	18	mA	
Input Pull-up Resistance PA, PB, PD, PE, PF, PC, PH, PI, PJ	R_{PU}	45	53	82	kΩ	V_{IN} = 0

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Pull-down Resistance PA, PB, PD, PE, PF, PC, PH, PI, PJ	R_{PD}	37	49	91	kΩ	$V_{IN} = V_{IO\_VDD}$
Input Pull-up Resistance nRESET	R_{RST}	45	53	85	kΩ	

Note:

1. nRESET pin is a Schmitt trigger input.

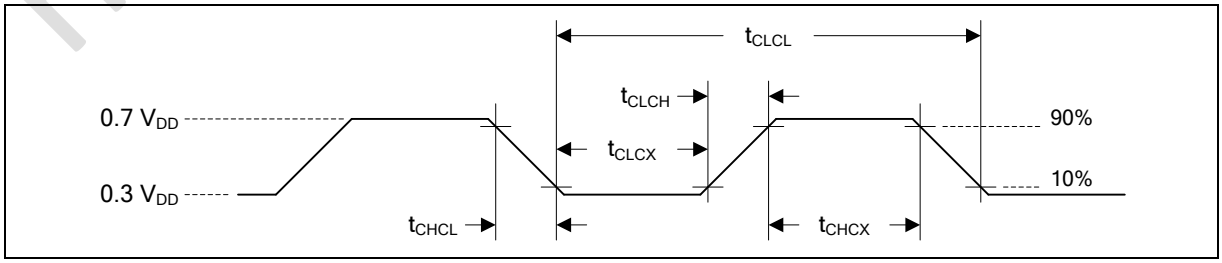
2. Pins of PA, PB, PD, PE, PF, PG, PH, PI and PJ can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=3.63 V, the transition current reaches its maximum value when V_{IN} approximates to 1.5 V.

7.3 AC Electrical Characteristics

7.3.1 External 4~24 MHz High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	20	-	-	ns	-
t_{CLCX}	Clock Low Time	20	-	-	ns	-
t_{CLCH}	Clock Rise Time	-	-	10	ns	-
t_{CHCL}	Clock Fall Time	-	-	10	ns	-

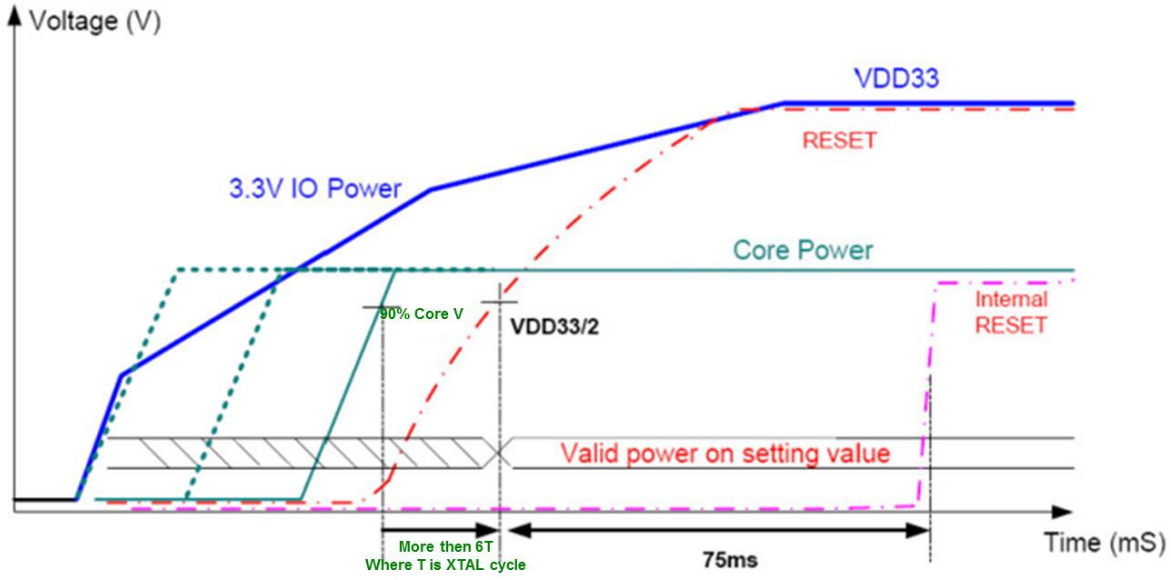
Note. Using 12MHZ is suggestion.



Note: Duty cycle is 50%.

Figure 7.3-1 External 4~24 MHz High Speed Oscillator Timing Diagram

7.3.2 Power-on Sequence & RESET



7.3.2.1 Power up Sequence

- Higher Voltage (3.3V) First
- Sequence: T33 ≥ T18 ≥ T12, (The time delay gap between < 1mS is prefer, typical 0mS is recommend)

7.3.2.2 Power down Sequence,

- The lower voltage (1.2V) should be powered down first and then the higher one (3.3V)
- Sequence: T12 ≥ T18 ≥ T33

Note.

- T12 represents 1.2V powered time for Core power
- T18 represents 1.8V powered time for MVDD power
- T33 represents 3.3V powered time for I/O power

7.3.3 External 4~24 MHz High Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.97	3.3	3.63	V	-
T_A	Temperature	-40	-	85	°C	-
f_{HXT}	Clock Frequency	4	-	24	MHz	-

7.3.3.1 Typical Crystal Application Circuits

Crystal	ESR (ohm)	C1, C2
4M ~ 8M	< 100	20 pf
8M ~ 18M	< 50	14 pf
18 MHz ~ 24 MHz	< 30	8 pf

Note. XTAL 12MHz is suggestion.

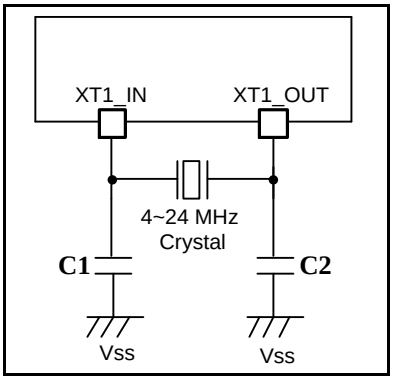


Figure 7.3-2 Typical HXT Crystal Application Circuit

7.3.4 External 32.768 kHz Low Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{LXT}	Operation Voltage	2.97	3.3	3.63	V	-
T_A	Temperature	-40	-	85	°C	-
f_{LXT}	Clock Frequency	-	32.768	-	kHz	-

7.3.4.1 Typical Crystal Application Circuits

Crystal	C1	C2
32.768 kHz	20pf	20pf

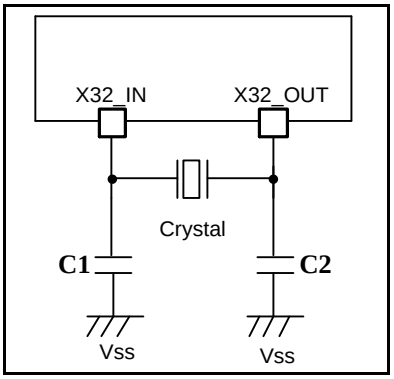


Figure 7.3-3 Typical LXT Crystal Application Circuit

7.3.5 I²C Interface Timing

Symbol	Parameter	100K		400K		Unit	Test Condition
		Min	Max	Min	Max		
T_{LOW}	I2C_SCL Low Period	4.7	-	1.2	-	us	-
T_{HIGH}	I2C_SCL High Period	4	-	0.6	-	us	-
T_{SU_STA}	Repeated START Condition Setup Time	4.7	-	1.2	-	us	-
T_{HD_STA}	START Condition Hold Time	4	-	0.6	-	us	-
T_{SU_STO}	STOP Condition Setup Time	4	-	0.6	-	us	-
T_{BUF}	Bus Free Time	4.7	-	1.2	-	us	-
T_{SU_DAT}	Data Setup Time	2	-	0.3	-	us	-
T_{HD_DAT}	Data Hold Time	0	4.2	0	0.8	us	-
T_R	I2C_SCL/I2C_SDA Rise Time	-	1000	20+0.1Cb	300	ns	-
T_F	I2C_SCL/I2C_SDA Fall Time	-	300	-	300	ns	-
C_b	Capacitive Load for Each Bus Line	-	400	-	400	pF	-

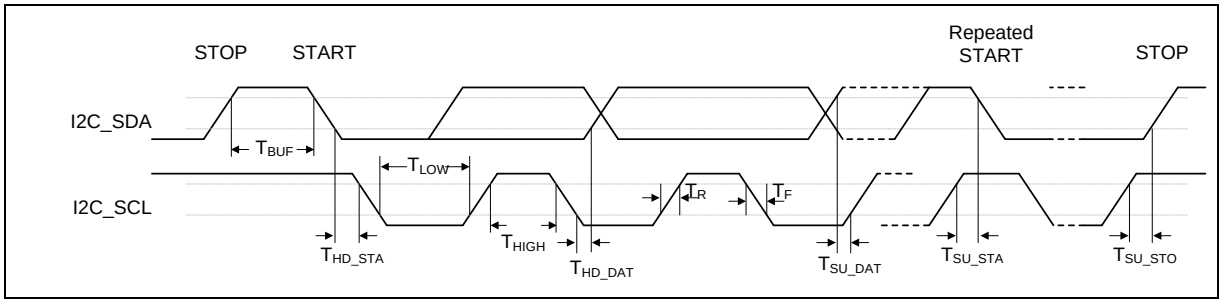


Figure 7.3-4 I²C Interface Timing Diagram

7.3.6 SPI Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SPI\_CLK}$	SPI_CLK Period	56	-	-	ns	-
$T_{H\_SPI\_CLK}$	SPI_CLK High Time	28	-	-	ns	-
$T_{L\_SPI\_CLK}$	SPI_CLK Low Time	28	-	-	ns	-
$T_{SU\_SPI\_DI}$	SPI_DI or SPI_DATA[3:0] Setup Time to SPI_CLK Active Edge	11	-	-	ns	-
$T_{HD\_SPI\_DI}$	SPI_DI or SPI_DATA[3:0] Hold Time from SPI_CLK Active Edge	1	-	-	ns	-
$T_{DLY\_SPI\_DO}$	SPI_CLK Active Edge to Valid SPI_DO or SPI_DATA[3:0] Delay	-	-	4	ns	-
$T_{HD\_SPI\_DO}$	SPI_DO or SPI_DATA[3:0] Hold Time from SPI_CLK Active Edge	0.2			ns	

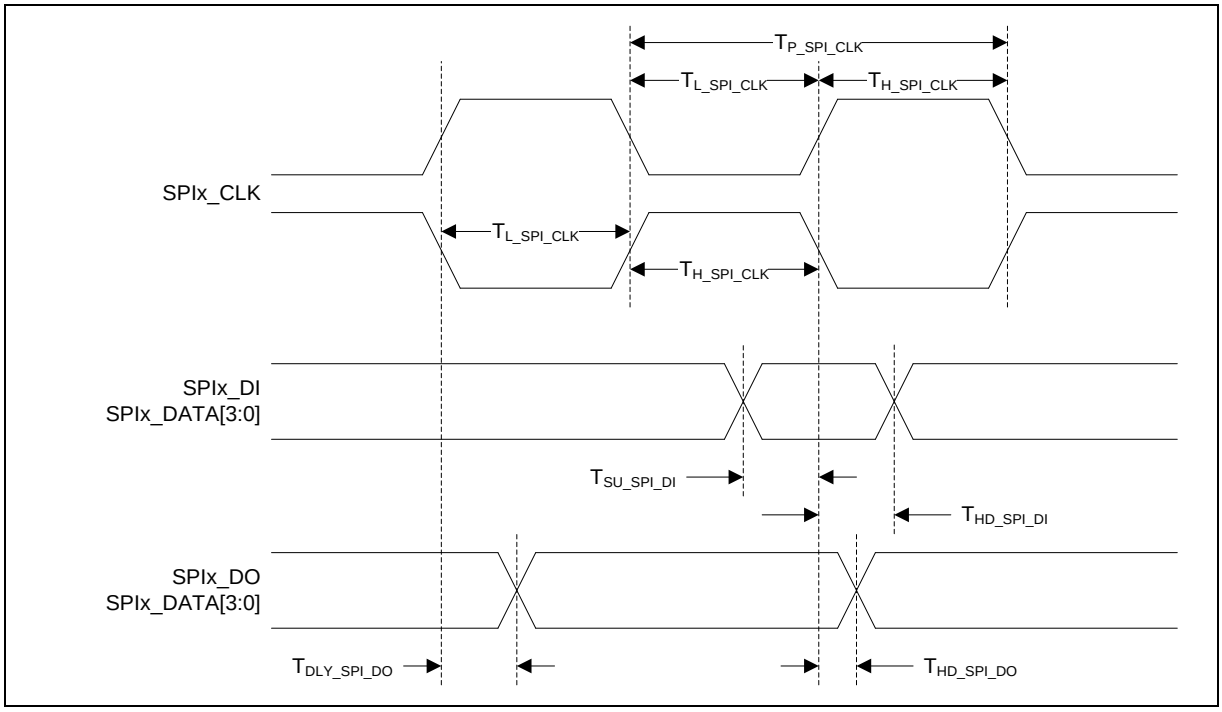


Figure 7.3-5 SPI Interface Timing Diagram

7.3.7 I²S Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_I2S\_BITCLK}$	I2S_BITCLK Period	50	-	-	ns	-
$T_{H\_I2S\_BITCLK}$	I2S_BITCLK High Time	25	-	-	ns	-
$T_{L\_I2S\_BITCLK}$	I2S_BITCLK Low Time	25	-	-	ns	-
$T_{DLY\_I2S\_DO}$	I2S_BITCLK Rising to Valid I2S_WS or I2S_DATAO Delay	-	-	6	ns	-
$T_{HD\_I2S\_DO}$	I2S_WS or I2S_DATAO Hold Time from I2S_BITCLK Rising	1	-	-	ns	
$T_{SU\_I2S\_DI}$	I2S_DATAI Setup Time to I2S_BITCLK Rising	5	-	-	ns	-
$T_{HD\_I2S\_DI}$	I2S_DATAI Hold Time from I2S_BITCLK Rising	3	-	-	Ns	-

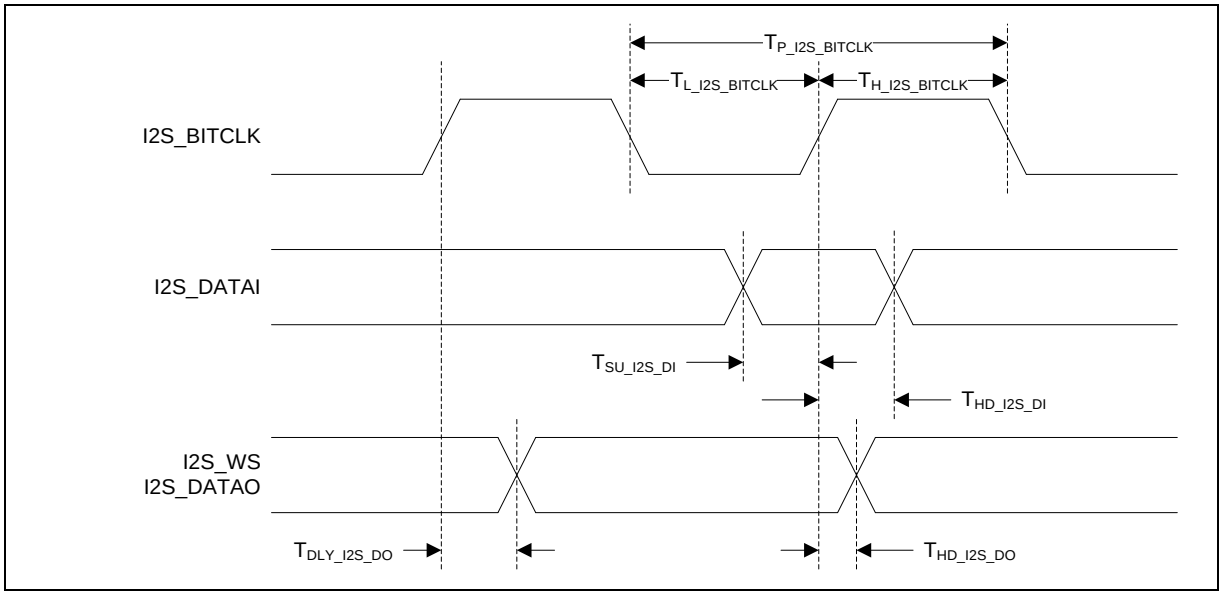


Figure 7.3-6 I²S Interface Timing Diagram

7.3.8 NAND Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{H\_NAND\_nWE}$	NAND_nWE High Time	-	15[1]	-	Ns	-
$T_{L\_NAND\_nWE}$	NAND_nWE Low Time	-	45[2]	-	ns	-
$T_{DLY\_DATA\_OUT}$	NAND_nWE Falling to Valid NAND_DATA Delay	-	15[3]-		ns	-
$T_{HD\_DATA\_OUT}$	NAND_DATA Hold Time from NAND_nWE Rising	7.5[3]	-	-	Ns	-
$T_{SU\_DATA\_IN}$	NAND_DATA Setup Time to NAND_nRE Rising	15[3]	-	-	ns	-
$T_{HD\_DATA\_IN}$	NAND_DATA Hold Time from NAND_nRE Rising	7.5[3]	-	-	ns	-

Note 1: NAND controller operating clock is 132 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.

Note 2: NAND controller operating clock is 132 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.

Note 2: NAND controller operating clock is 132 MHz

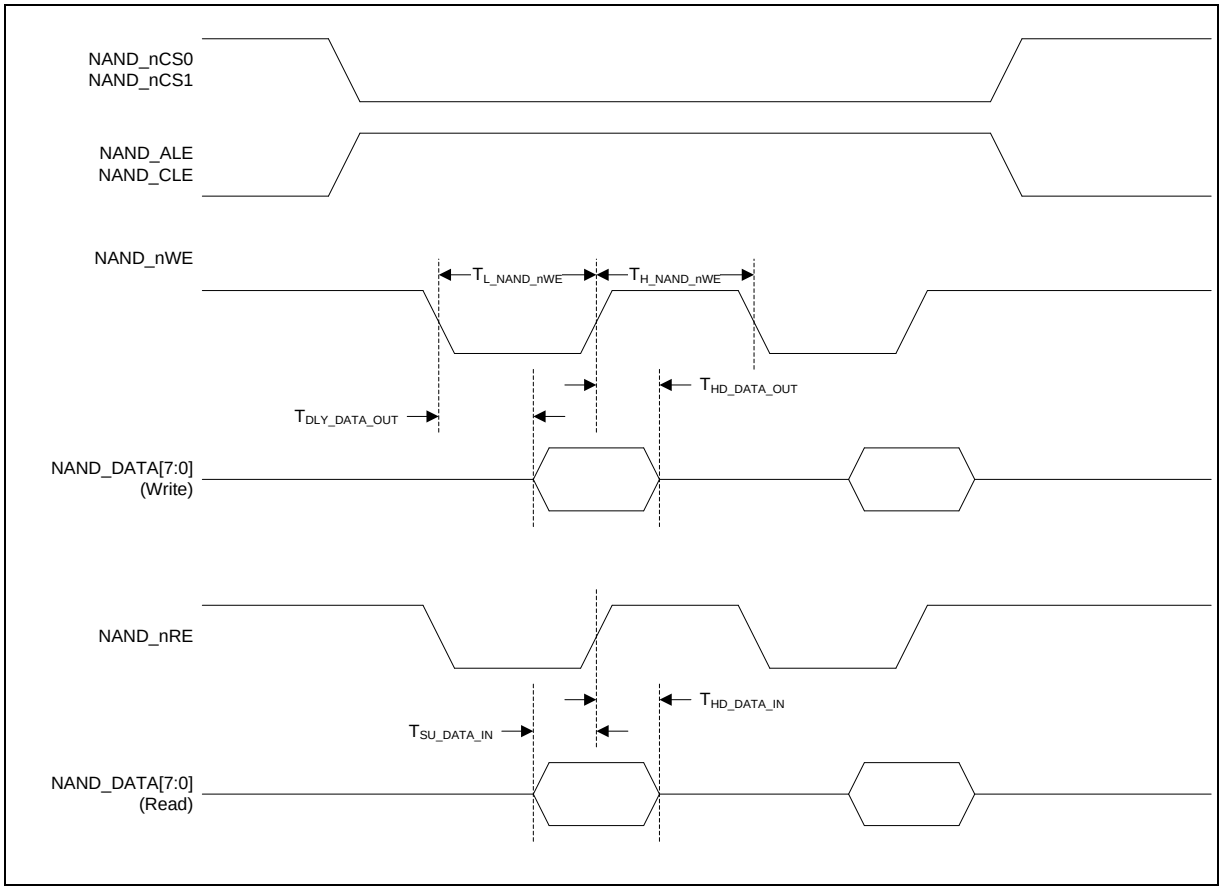


Figure 7.3-7 NAND Interface Timing Diagram

7.3.9 SD Interface Timing

7.3.9.1 Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

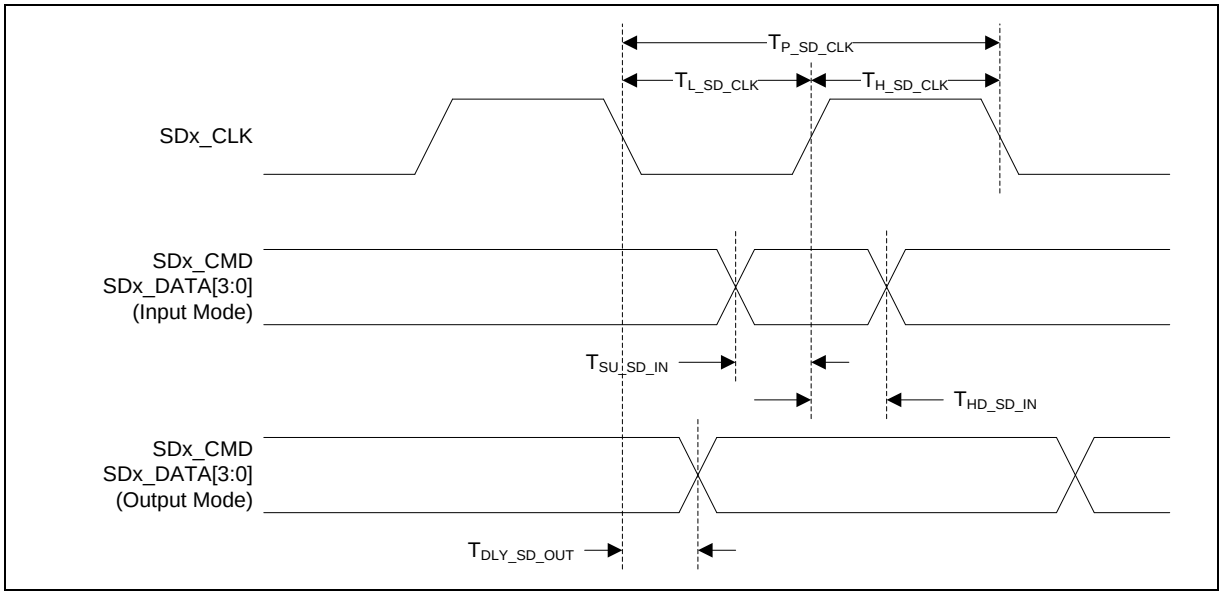


Figure 7.3-8 SD Interface Default Mode Timing Diagram

7.3.9.2 High-Speed Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

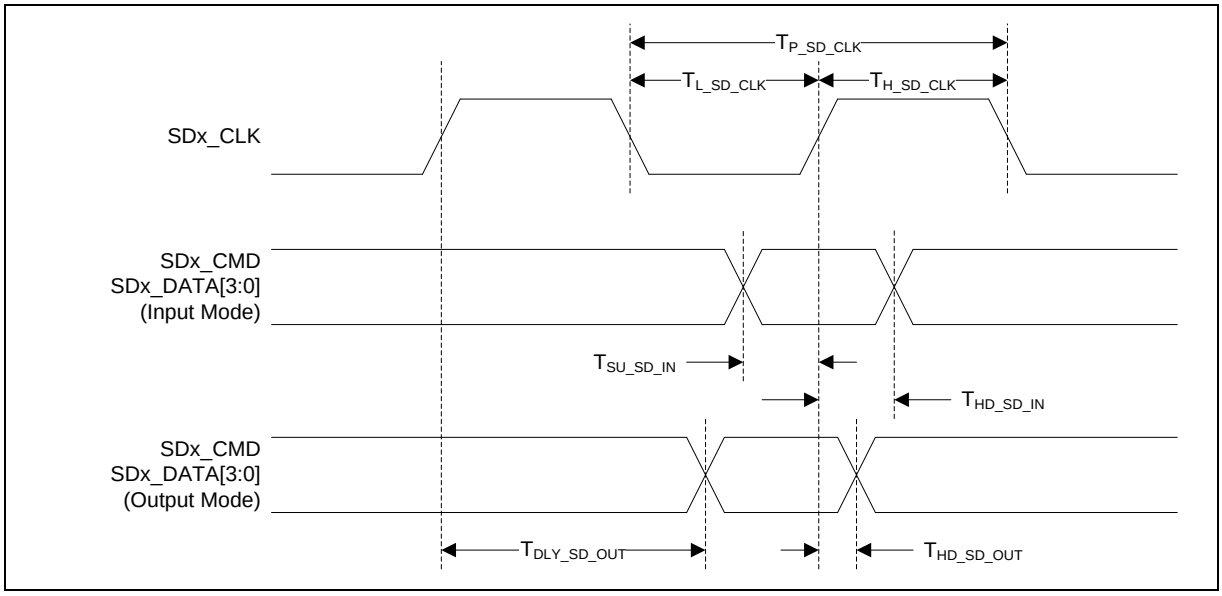


Figure 7.3-9 SD Interface High-Speed Mode Timing Diagram

7.3.10 LCD Display Interface Timing

7.3.10.1 SYNC Type Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_LCD\_CLK}$	LCD_CLK Period	13	-	-	ns	-
$T_{H\_LCD\_CLK}$	LCD_CLK High Time	6.5	-	-	ns	-
$T_{L\_LCD\_CLK}$	LCD_CLK Low Time	6.5	-	-	ns	-
$T_{DLY\_LCD\_OUT}$	LCD_CLK Rising to Valid LCD_HSYNC, LCD_VSYNC, LCD_DEN and LCD_DATA Delay	-	-	6	ns	-
$T_{HD\_LCD\_OUT}$	LCD_HSYNC, LCD_VSYNC, LCD_DEN and LCD_DATA Hold Time from LCD_CLK Rising	1	-	-	ns	-

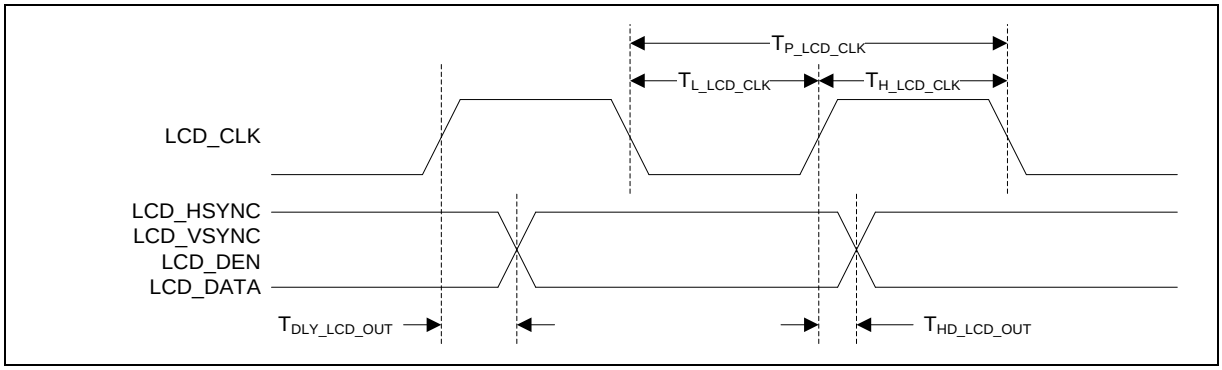


Figure 7.3-10 LCD Display Interface SYNC Type Timing Diagram

7.4 Analog Characteristics

7.4.1 12-bit SARADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{REF} is external AVREF pin
INL	Integral Nonlinearity Error	-	-1.2	-	LSB	V_{REF} is external AVREF pin
E_O	Offset Error	-	+3.7	-	LSB	V_{REF} is external AVREF pin
E_G	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V_{REF} is external AVREF pin
E_A	Absolute Error	-	4.2	-	LSB	V_{REF} is external AVREF pin
-	Monotonic	Guaranteed				
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	
T_{CAL}	Calibration Time	-	3	-	Clock	
T_S	Sample Time	-	17	-	Clock	
T_{ADC}	Conversion Time	-	20		Clock	
F_S	Sample Rate	-	-	800[1]	k SPS	
V_{AVDD}	Supply Voltage	2.7	3.3	3.6	V	
I_{DDA1}	Supply Current (Avg.)	-	1.2		mA	ADC channel 1 high speed mode
I_{DDA2}	Supply Current (Avg.)	-	1.0		mA	ADC channel 1 low speed mode
I_{DDA3}	Supply Current (Avg.)	-	0.4		mA	
I_{LK}	Leakage Current	-	0.1	-	uA	
V_{REF}	Reference Voltage	2	-	V_{AVDD}	V	
V_{IN}	Analog Input Voltage	0	-	V_{REF}	V	
R_{IN}	Analog Input Impedance	-	-	2	MΩ	
C_{IN}	Capacitance	-	25.6		pF	

Note:

1. ADC channel 1 supports sample rate higher than 160k SPS. Other ADC channels support sampel rate up to 160k SPS.

7.4.2 Low Voltage Detection (LVD) and Low Voltage Reset (LVR)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{DD}	Operation Voltage	2.0	3.3	3.63	V	-
I_{DD}	Operating Current		21		uA	-
I_{LK}	Quiescent Current	-	0.1	0.5	uA	LVR_EN (SYS_LVRDCR[0]) = 0, LVD_EN (SYS_LVRDCR[8]) = 0
T_A	Temperature	-40	-	85	°C	-
V_{TH_LVD}	LVD Threshold Voltage	2.295	2.55	2.805	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		2.475	2.75	3.025	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{TH_LVR}	LVR Threshold Voltage	2.115	2.35	2.585	V	-
V_{HY_LVD}	LVD Hysteresis	0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{HY_LVR}	LVR Hysteresis	0.045	0.05	0.055	V	-

7.4.3 3.3V Power-On Reset (POR33)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	125	°C	-
V_{POR}	Reset Voltage	-	1.83	-	V	AVDD rising from 0V to 3.3V
I_{POR33}	Quiescent current	-	5	-	nA	Vin > reset voltage

7.4.4 1.2V Power-On Reset (POR12)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	125	°C	-
V_{POR}	Reset Voltage	-	0.76	-	V	CORE_VDD rising from 0V to 1.2V
I_{POR12}	Quiescent current	-	10	-	nA	Vin > reset voltage

7.4.5 USB 2.0 PHY

7.4.5.1 Low/Full-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OL}	Output Low (Driven)	-	-	0.3	V	1.5K RPU on DP to 3.6v
V_{OH}	Output High (Driven)	2.8	-	-	V	15K RPD on DP, DM to GND
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	$\|V_{USB0\_DP}–V_{USB0\_DM}\|$
V_{CM}	Differential Common-Mode Range	0.8	-	2.5	V	
V_{IL}	Single-Ended Input Low	-	-	0.8	V	-
V_{IH}	Single-Ended Input High	2.0	-	-	V	-
R_{PU}	Pull-Up Resistor	1.35	1.5	1.65	kΩ	
R_{PD_DP}	D+ Pull-Down Resistor	13.5	15	16.5	kΩ	
R_{PD_DM}	D- Pull-Down Resistor	13.5	15	16.5	kΩ	
Z_{DRV}	Driver Output Resistance	28	-	44	Ω	Steady state drive[1]

Note:

1. Driver output resistance doesn't include series resistor resistance.

7.4.5.2 High-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HSDI}	High Speed Differential Input Signal Level	150	-	-	mV	$\|V_{USB0\_DP}-V_{USB0\_DM}\|$
V_{HSQ}	High Speed Squelch Detection Threshold	100	125	150	mV	$\|V_{USB0\_DP}-V_{USB0\_DM}\|$
V_{HSCM}	High Speed Common Mode Voltage Range	-50	-	500	mV	
V_{HSOH}	High Speed Data Signaling High	300	400	440	mV	
V_{HSOL}	High Speed Data Signaling Low	-10	0	10	mV	
V_{CHIRPJ}	Chirp J Level	700	-	1100	mV	
V_{CHIRPK}	Chirp K Level	-900	-	-500	mV	
R_{HSDRV}	High Speed Driver Output Resistance	40.5	45	49.5	Ω	

7.4.5.3 USB Low-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{LRISE}	Rise Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
T_{LFALL}	Fall Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{LCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

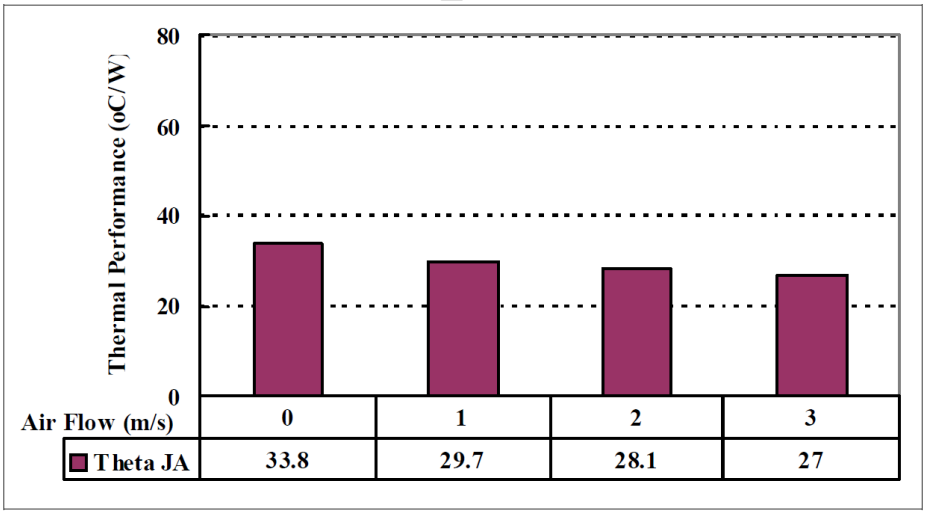
7.4.5.4 USB Full-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FRISE}	Rise Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FFALL}	Fall Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

7.4.5.5 USB High-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRISE}	High Speed Driver Rise Time	500	-	900	ps	CL<10pF
V_{HFALL}	High Speed Driver Fall Time	500	-	900	ps	CL<10pF

7.5 Thermal Characteristics of N9H30 Package



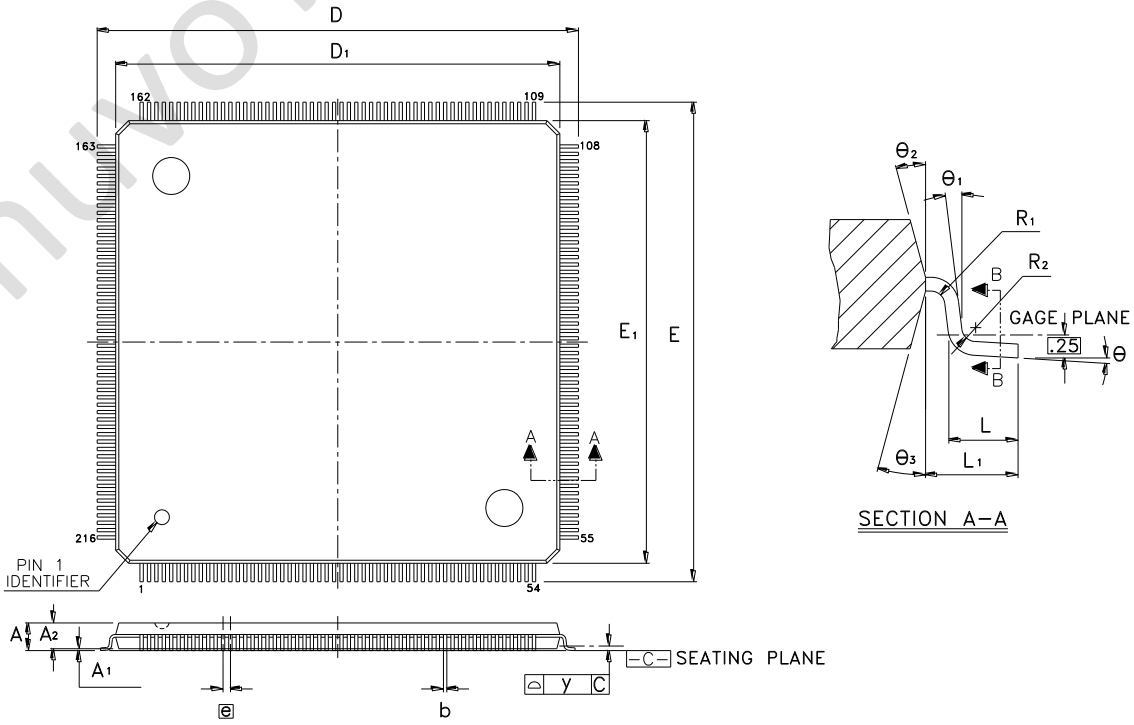
Thermal Performance of SLQFP under Forced Convection

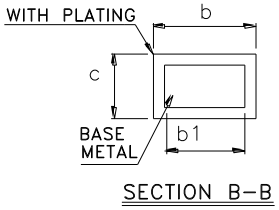
7.5.1 Simulation Conditions

Input Power	Top die: 0.6 W Bottom die: 0.6W
Test Board (PCB)	4 layers
Control Condition	Air Flow = 0,1, 2, 3 m/s

8 PACKAGE DIMENSIONS

8.1 216L LQFP (24x24x1.4mm footprint 2.0mm)

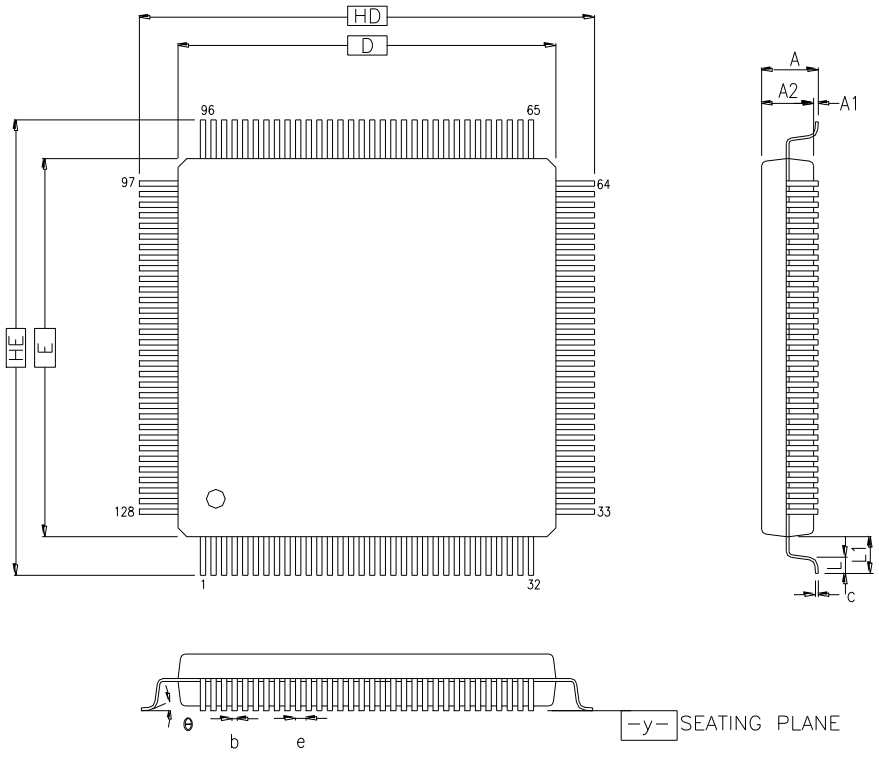




Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
y	0.08			0.00314		

8.2 128L LQFP (14x14x1.4mm footprint)

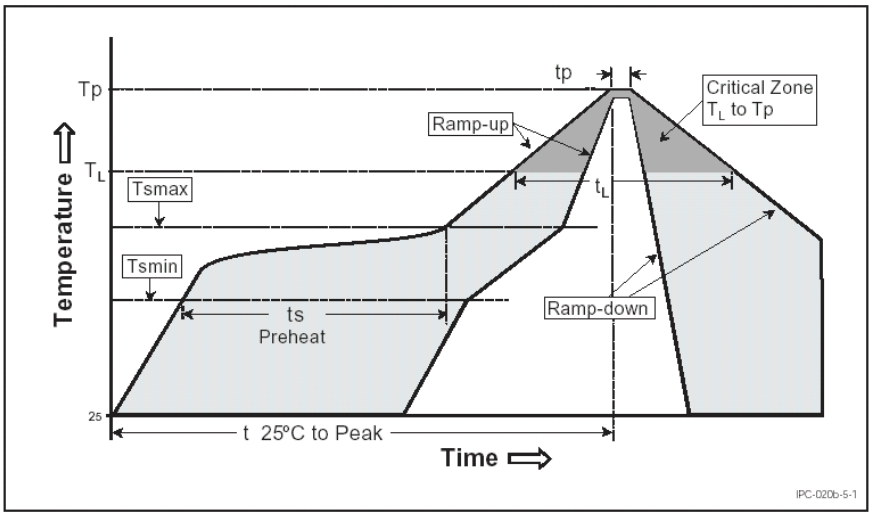


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8.3 PCB Reflow Profile Suggestion

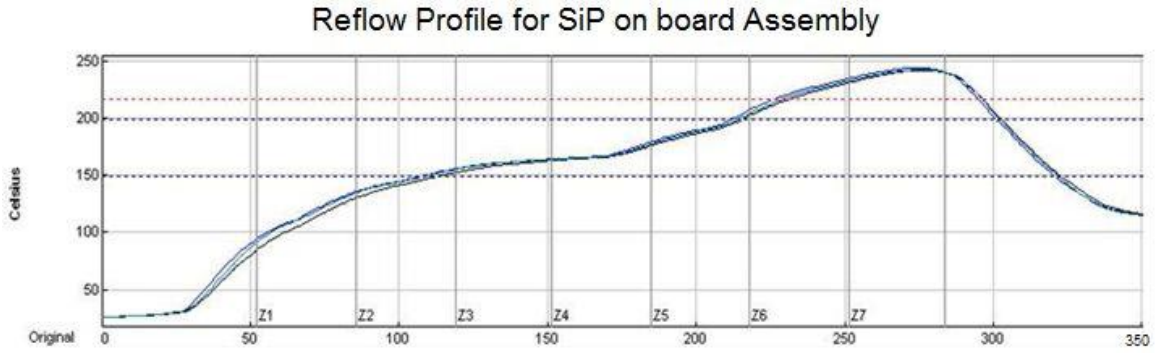
8.3.1 Profile Setting Consideration



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_p)	< 3℃/second		< 3℃/second	
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	100℃ 150℃ 60-120 seconds		150℃ 200℃ 60-180 seconds	
Time maintained above: -Temperature (T_L) -Time (t_L)	183℃ 60-150 seconds		217℃ 60-150 seconds	
Peak Temperature (Tp)	225+0/-5℃		245+5/-5℃	
Time within 5℃ of actual Peak Temperature (tp)	10-20 seconds		10-30 seconds	
Ramp-down Rate	3℃/second max.		3℃/second max.	
Time 25℃ to Peak Temperature	6 minutes max.		8 minutes max.	

Note: 1.All temperatures refer to topside of the package, measured on the package body surface.
2.Depends on other parts on board density and follower solder paste manufacturers's guidelin

8.3.2 Profile Suggestion for N9H30 series



Preheat time	150℃—200℃: 105+/-15sec
Dwell time	Over 220℃: 70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp Up/Down Rate	Up: 3 +0/-2 ℃/ sec Down: 2 +0/-1℃/ sec

9 REVISION HISTORY

Date	Revision	Description
2018,05,16	1.00	1. Preliminary version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.